ULTRA HIGH SPEED IMAGE PROCESSING TECHNIQUES

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April 1981
Final Report

Prepared for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

(NASA-CR-166771) ULTRA HIGH SPEED IMAGE PROCESSING TECHNIQUES Final Report (General Electric Co.) 75 p HC A04/MF A01 CSCL 09C

N82-19466

Unclas
G3/33 09227

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INTRODUCTION

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INTRODUCTION

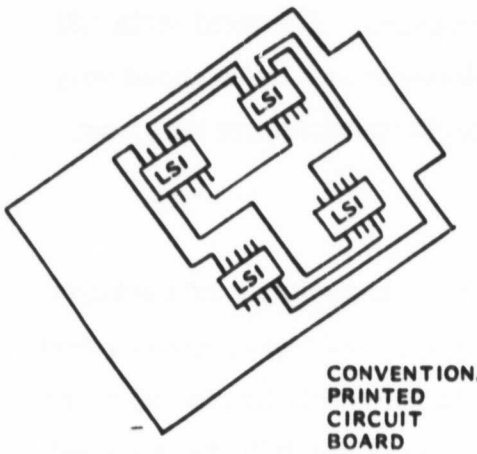
In answer to the increasing need for high speed sensor data processing in flight spacecraft, NASA, Goddard Space Flight Center is pursuing the development of the Massively Parallel Processor (MPP) [1,2,3]. The MPP is configured with thousands of parallel processing elements implemented with Large Scale Integrated (LSI) circuit techniques. The solid state LSI technology for the development of these high speed processing elements is moving ahead very rapidly, spurred on by the commercial market needs for more logic operations at less cost, power and improved reliability.

One area receiving little attention is how are these LSI circuits to be assembled and packaged together to form the overall MPP. As LSI circuit element geometries decrease, speed/power improvements are achieved which translates into improvements in reliability by placing more function and high speed functions on a single silicon die. This means fewer IC's/function and lower operating temperature. Both of these result in lower cost and greater reliability.

However, these LSI solid state developments to finer geometries do not address one basic problem; and that is, how do we package these LSI's together? The old presently accepted printed circuit board approach to mounting and interconnecting LSI circuits results in relatively long LSI circuit interconnecting lines. These lines in this planar packaging approach have significant capacitance which must be driven by the LSI circuitry. The resultant LSI output buffers must be large in size to drive this line capacitance which tends to slow down the circuitry on the LSI circuit as well as significantly increasing the power dissipation. This leads to more parallel LSI circuits to maintain the parallel processor throughput as well as greater processor power dissipation which adds to the problem of removing that heat from the processor. In addition, cost is increased due to the cost of generating the relatively high operating power on board the spacecraft.

To significantly reduce these problems, the LSI circuit interconnection capacitance must be reduced. One way of accomplishing this is to stack the LSI circuits together in a 3-dimensional module rather than lay them out on a planar surface, see Figure. With this approach the

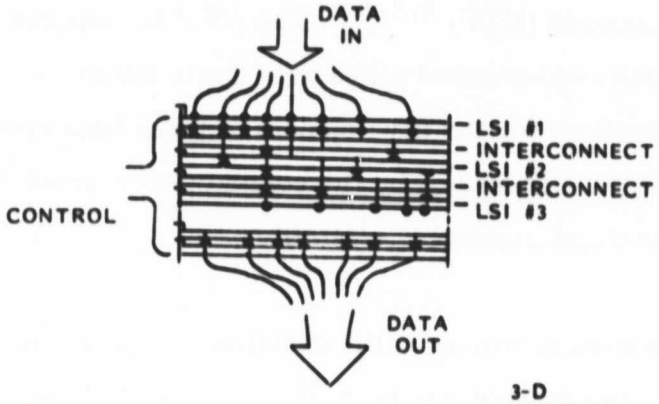
interconnection path lengths reduce to tenths of inches, rather than inches, for an order of magnitude reduction in interconnection capacitance. This study contract worked on the development of 3-dimensional stacked packaging techniques for CMOS on sapphire LSI circuits.



CONVENTIONAL PRINTED CIRCUIT BOARD

- o INTERCONNECTING RUNS BETWEEN LSI CIRCUITS ARE INCHES LONG. THEREFORE PARASITIC CAPACITANCES = PICCOFARADS

2 DIMENSIONAL LSI PACKAGING



3-D STACKED LSI

- o INTERCONNECTING RUNS BETWEEN LSI CIRCUITS ARE TENTHS OF INCHES LONG. THEREFORE PARASITIC CAPACITANCES = TENTHS OF PICCOFARADS

TENTHS OF INCHES

- HIGHER SPEED 10 TO 1
- REDUCED POWER 3 TO 1
- REDUCED LSI CHIP AREA (15% SAVINGS)
- REDUCED NO. OF INTERCONNECTIONS 3 TO 1

3 DIMENSIONAL LSI PACKAGING

LSI/VLSI Packaging

Silicon on Sapphire (SOS) was chosen as the LSI technology because of its inherent fast operating circuit speeds and low operating power. In addition, sapphire is an insulator which makes it a good candidate for implanting isolated conductive feedthroughs through the substrate. The program was divided into three tasks. Task I developed hole drilling techniques for an array of holes through sapphire substrates. Task II developed techniques to implant feedthrough conductors through the drilled holes in the sapphire substrates. Task III developed a custom LSI circuit and demonstrated the ability to connect the feedthrough conductors to the custom CMOS/SOS LSI circuitry on the substrate.

SECTION 2

SUMMARY

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SUMMARY

This program had as its objective to develop advanced 3-dimensional packaging techniques for ultra high speed imaging techniques that would minimize the interconnection line lengths between LSI circuits and thereby reduce the parasitic capacitance effects by an order of magnitude. The approach to accomplishing this was to develop techniques for implanting conductive feedthroughs through silicon on sapphire LSI circuitry, so that LSI sapphire substrates could be stacked and directly connected together, one on top of the other, Figure 1.

To form feed-through conductors in SOS required successful completion of 3 tasks, namely:

1. Drill suitably aligned small holes in SOS without damaging the sapphire substrate.
2. Implant a conductor in the holes in the sapphire substrate with an essentially 100% implant yield.
3. Form interconnecting conduction paths between feed-through conductors on the top and bottom face of the wafer by double-sided photo-lithographical techniques.

Task I - Hole Drilling

Three methods were tried for making holes in SOS, Silicon on Sapphire LSI substrates. These methods were ultrasonic drilling, electron beam drilling and laser drilling. Ultrasonic drilling was dismissed as a candidate because it was incapable of producing holes with aspect ratios of greater than 2:1 at the hole sizes required for feedthroughs. Electron beam drilling was capable of making holes but the beam pulse could not be made sufficiently short so that heating and cracking of the sapphire could be avoided.

Laser drilling was selected as the best available method for drilling holes in SOS. Extensive laser drilling tests were run on pulsed, CW and Q-switched lasers at Laser Applications Inc., U.S. Laser Corp., Raytheon, General Photonics, Lasermation, GE, Solid State Applications Operation, GE-Valley Forge Space System Division and GE-Corporate Research Center. CW and pulsed lasers cracked the SOS wafers. Q-switched lasers with the proper power, pulse length and number of pulses produced holes ranging from 1/2 to 5 mils in diameter. In general,

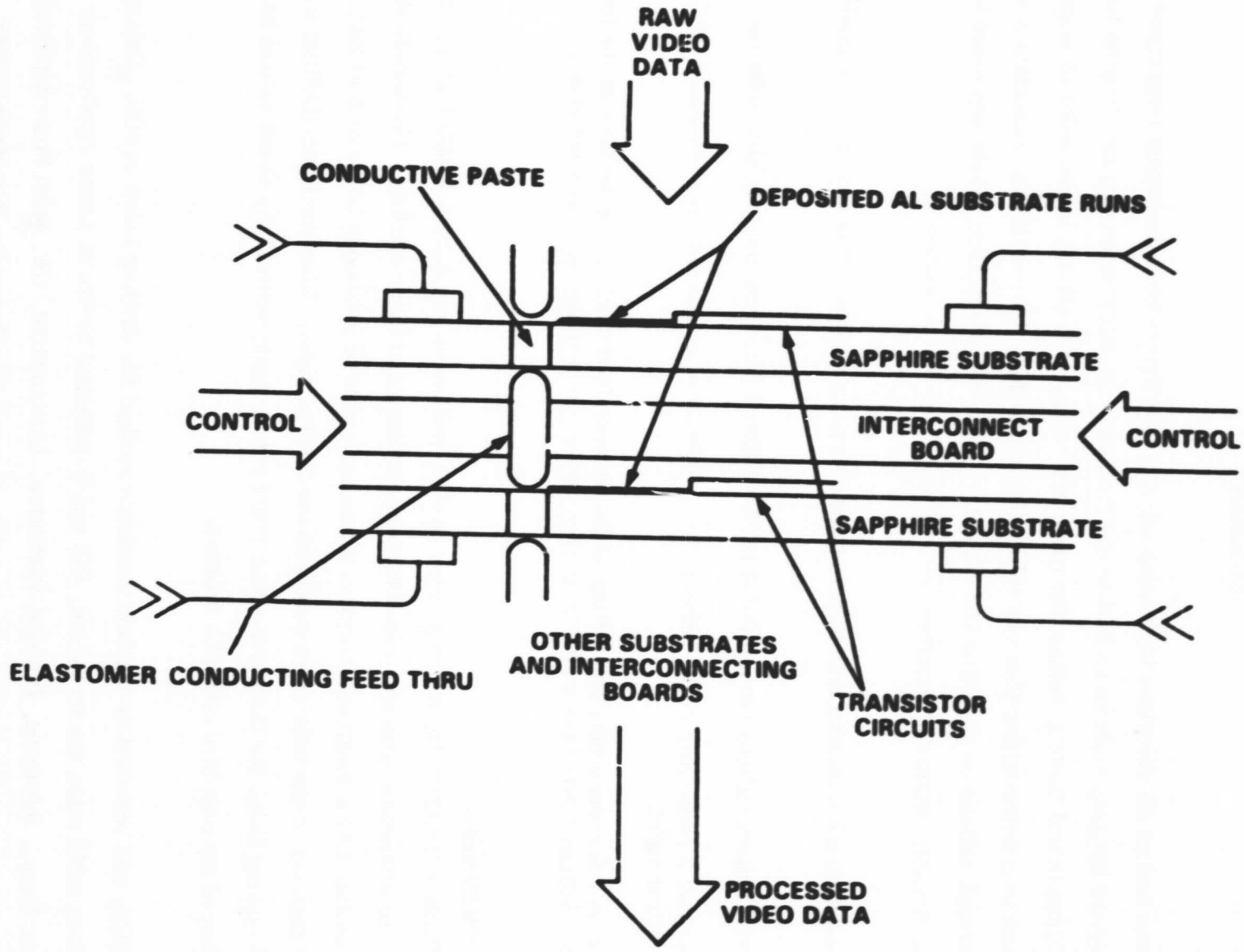

Figure 1. Ultra High Speed Image Processing LSI

it was found that the holes drilled with the laser had a small random offset which could be cured by limiting the number of separate pulses used for drilling. Also, it was found that at intermediate power levels, the laser could be made to drill in a reverse mode, that is, from the back surface to the front surface of the SOS substrate. This reverse mode had the advantage that debris from the drilling was ejected from the rear of the wafer so that damage to the microelectronic circuits on the front face of the wafer was minimized.

Task II

In parallel with the laser drilling activities, a number of methods were tried to implant conductors in the laser-drilled holes in the SOS wafer. The method which gave a 100% implant yield was used on the final wafers. This method was the double-sided and through-hole electroplating technique. It involved sputtering metal on both faces of the wafer to form an electrical feedthrough with a resistance of 30,000 ohms. This resistance was lowered to 10^{-4} ohms by a subsequent through hole electroplating treatment.

Task III

A custom CMOS/SOS LSI circuit was designed and produced that contained pads for feedthrough holes at various spacings and at various spacings relative to aluminum runs and active CMOS inverters. Spacings as close as 0.2 mil and as far apart as 20 mils were incorporated into the layout design. Sample wafers were processed, covered with a protective layer of glass and then a layer of photo resist. Windows were opened in the glass and photo resist layered at points where holes were to be laser drilled through the wafer. Holes were then laser-drilled at these points and were enlarged to a standard 2 mil hole size by a laser reaming technique.

With these final wafers, it was decided to try a new twist to the sputtering technique by sputtering two layers of metal onto the wafer. The first layer was NiCr which was used to form a tenacious bond with the sapphire substrate and to form a barrier layer between the aluminum runs and the second sputtered layer of gold. This barrier layer is advantageous if the wafer is to be later heated to high temperatures to prevent the formation of gold-aluminum intermetallic compounds more commonly known as the purple plague.

Following deposition of these layers on both sides of the wafer, the wafer was placed in an electroplating bath where a layer of copper was plated onto the wafers and in the laser-drilled holes.

The wafers were then sent to the photolithography unit to remove the sputtered and electroplated metal from the major faces of the wafer. Previously tests had been run with dummy wafers that showed that the sputtered and electroplated layers could be removed by a common photo-resist lift-off techniques. With all of the experiments being run in parallel the initial lift-off experiments were done with wafers that were laser-drilled with a different laser than was used to drill the final wafers. It was found with the final wafers, that there was difficulty with the lift-off technique. The laser that was used on the final wafers had a slightly larger divergence than the laser used on the test photolithography wafers with the result that the photo-resist around the hole was cautherized to the point that it would not lift off.

As a backup to photo-resist lift-off, removal of the metal from the wafer faces by selective etches was tried. The NiCr layer proved to be the Achilles heel of this effort since any etch that would remove NiCr also removed the underlying layer of Al, thereby destroying the pad connecting the feedthrough to the Al run. This problem can be easily avoided in the future by not using a NiCr layer since the wafer can be kept below temperatures where the purple plague appears. Then, with just a gold layer overlying an aluminum layer, the gold layer can be removed by a selective etch that does not attack the aluminum layer. Alternatively, an extra mask can be fabricated that will allow one to deposit a protective layer of photo-resist over the feedthrough pad locations to protect them from etching when the sputtered metal film is being removed from the rest of the top and bottom surfaces of the SOS wafer.

SECTION 3

HOLE DRILLING THROUGH SAPPHIRE LSI CIRCUIT SUBSTRATES

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HOLE DRILLING THROUGH SAPPHIRE LSI CIRCUIT SUBSTRATES

3.1 HOLE DRILLING THROUGH SAPPHIRE

3.1.1 SURVEY OF DRILLING TECHNIQUES

Three promising techniques were examined as possible means to drill holes through SOS. These were ultrasonic drilling, electron beam drilling and laser drilling.

Ultrasonic drilling was eliminated quickly becasue it was only capable of making holes with a maximum depth-to-diameter ratio of two. In addition, ultrasonic drilling was the slowest of the three techniques examined. Drilling speed was an important criterion for rejection of the technique since up to one million holes per wafer may be needed by the massively parallel processor.

The second technique, electron beam drilling was fast. However, cracking of the SOS wafer was found around the electron beam drilled hole. This cracking resulted from thermal stresses caused by heating of the sapphire by the electron beam around the hole. Even with the minimum duration electron beam pulse, enough time elapsed to allow heat to diffuse into the sapphire which caused stresses and cracking. Because the electron beam pulse length could not be reduced below the critical relaxation time associated with heat diffusion stresses, this technique was abandoned in favor of laser drilling which had a much shorter pulse length than electron beam drilling.

3.1.2 LASER DRILLING THROUGH SAPFHIRE

3.1.2.1 Selection of Laser Technique

Two types of lasers and three laser operating modes were examined for laser drilling of the SOS wafers. Both CO_2 and NdYAG lasers successfully drilled SOS. A CO_2 laser has the advantage that its 10.2 micron wavelength is absorbed by sapphire. On the other hand, the relatively long wavelength of a CO_2 laser implies that the hole size obtainable by drilling will not be as small as with NdYAG. The disadvantage of NdYAG laser is that sapphire is almost

transparent to the 1.06 micron wavelength of NdYAG. However, this lack of absorbancy can be overcome by using a giant laser pulse to lead the train of pulses to be used for drilling. This leading giant pulse causes the temperature and thus the absorbtion coefficient of sapphire to increase to the extent where a following train of smaller pulses can drill the SOS wafer.

Three laser operating modes were tried for drilling SOS, namely, continuous wave (CW), pulsed and Q-switched. CW and pulsed modes caused cracking of the SOS wafers becasue of excessive heat diffusion into the sapphire substrate. The Q-switched mode, on the other hand, with its 200 nanosecond pulse length did not allow enough time for heat to diffuse into the sapphire substrate and cause thermal stresses and cracking. Consequently, a NdYAG Q-switched laser was selected as the drilling tool.

3.1.2.2 Random Walk of a Drilling Laser Beam

Forward laser drilling of sapphire was accomplished with SOS wafers mounted on a vacuum chuck which, in turn, was mounted on the bed of a movable x-y table. The flatness of the chuck surface was at $\pm$ 8μ over the area of the wafer. The laser working depth of focus was estimated experimentally to be about 100μ. The laser[4] was a frequency-doubled Q-switched NdYAG type (0.532μ) and was operated at integrated outputs of 300 and 450 mW in two separate series of experiments. The laser was pulsed electroncally at 1000 Hz. The horizontal pulsed beam was reflected downwards with a 45^{o} mirror through an adjustable beam expander. The collimated beam was focused on the inactive uncoated SOS-wafer surface that was facing upwards. Pulse duration was (100-110) x 10^{-9} sec. Although the energy per pulse was not measured, the peak power was estimated at 3 and 4.5 kW for the two series of experiments run at integrated powers of 300 and 450 mW, respectively.

During drilling operations, the x-y table bed was moved in a series of steps along the x direction and about 30 holes were drilled at approximately equal 100-μ separations along this line. At each hole, the beam was focused on the entrance surface. The time required to drill each hole was about 1 sec at 1000 pulses at 300 mW and about 0.8 sec at 1000 pps at 450 mW.

Following laser drilling, the SOS wafer was removed from the chuck and placed in a shallow Petri dish filled with silicone oil. The silicone oil was used to increase the light transmission

coefficient through the backside of the SOS wafer that has an etched and slightly frosted appearance. Photomicrographs of both sides of the SOS wafer were than taken with a transmission microscope with the microscope focused first on one side of the wafer and then immediately after focused on the other face of the wafer so as to obtain superimposed pictures of the positions and sizes of the exits and entrances of the laser drilled holes. Each photomicrograph contained images of nine holes.

3.1.2.2.1 Experimental Results

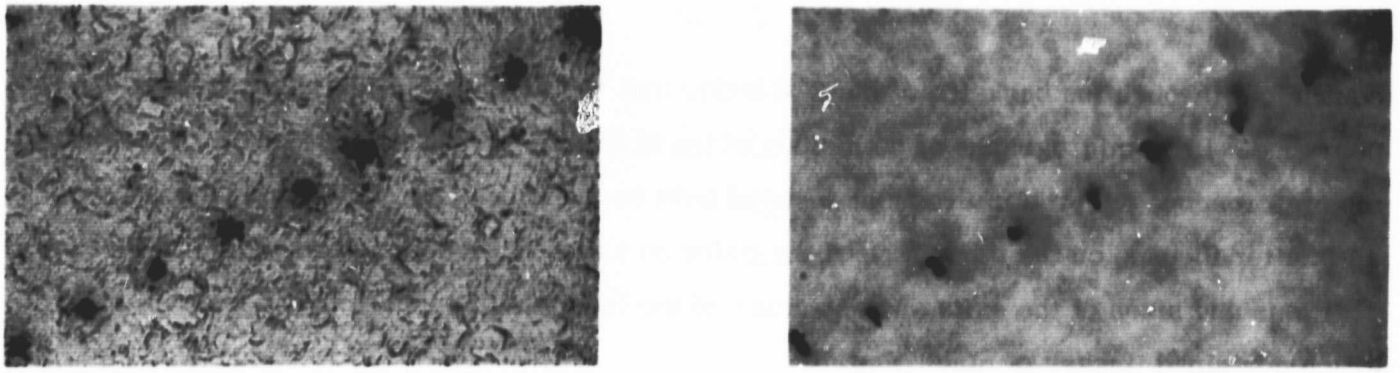
At an integrated power level of 300 mW, the holes had an entrance diameter of 10μ and an exit diameter of 6μ. Since the SOS wafer was 330μ thick, the holes had an average aspect ratio of 40 at 300 mW. At an integrated power level of 450 mW, the entrance-hole diameter was 18μ and the exit-hole diameter was 9μ, to give an average aspect ratio of 24.

Some spraying of debris was noted around the entrance hole forming a halo with a diameter of 45μ at 300 mW and 60μ at 450-mW power levels. On the exit surface the diameters of the spray halos were 15 and 21μ for the 300 and 450 mW power levels, respectively. No cracking or spalling of the sapphire or the epitaxial silicon layer was seen in these experiments.

No strain and thus no stress was detectable around the laser-drilled holes using optical inspection with a transmission microscope and a cross polarized (sapphire is birefringent).

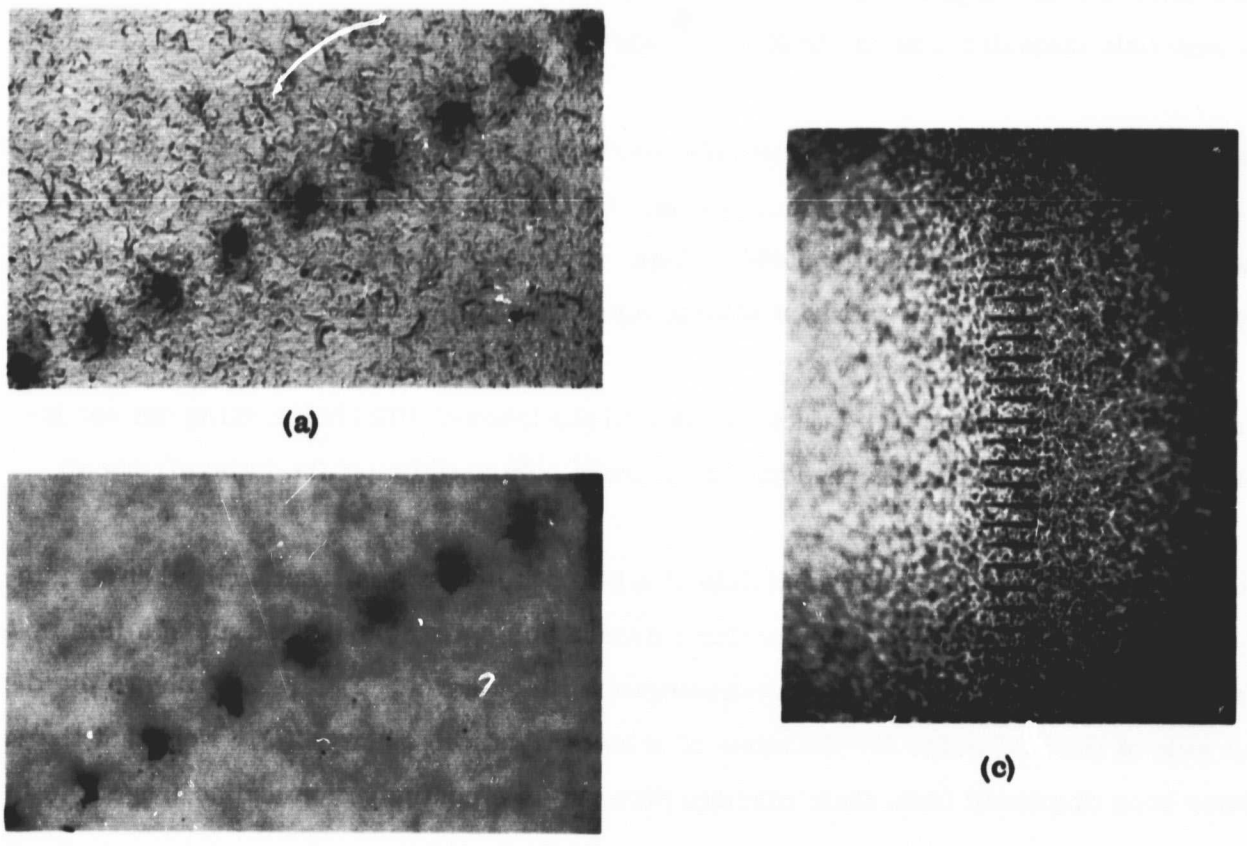
Figure 2(a) shows the drilling-entrance side of a SOS wafer that was laser drilled at an integrated power level of 300 mW. Because the entrance holes were positioned along a line by the x-y table bed, the nine holes in the microphotograph lie on a line. Figure 2(b) shows the drilling-exit side of the SOS wafer for the same nine holes shown in Figure 2(a). Note that the exit holes have been displaced from their original straight-line configuration and no longer lie in a linear array.

As shown in Figures 3(a) and 3(b), a similar displacement of the exit holes from an initial linear configuration is also observed when the pulsed laser is drilling at an integrated power level of 450 mW.



(a) (b)

Figure 2(a). The drilling-entrance side of an SOS wafer in which a series of holes lying along a straight line were drilled by a pulsed NdYAG laser operating at 1000 pulses/sec at an integrated pow[illegible] level at 300 mW (360x). (b) The drilling-exit side of an SOS wafer showing the same area shown in Figure 2(a). Note that the exit holes no longer lie along a straight line (360x).



(a) (c)

(b)

Figure 3(a). The drilling-entrance side of an SOS wafer in which a linear array of holes were drilled by a pulsed NdYAG laser operating at an intergrated power level of 450 mW and a cycle time of 1000 pulses/sec (360x). (b) The drilling-exit side of an SOS wafer showing the same area shown in Figure 2(a). The exit positions of the laser drilled holes no longer lie along a straight line (360x). (c) A view perpendicular to the laser-drilled holes shown in Figures 3(a) and 3(b). The holes are tapered so that the entrance diameter exceeds the exit diameter.

Although superimposed microphotographs were taken of both the entrance and exit holes without moving the specimen or changing the magnification of the microscope, exact superposition was not expected in even the ideal case of perfectly straight holes. The lack of superposition in even the ideal case stems from the difference of index of refraction between silicone oil and sapphire. This difference in refraction indexes causes objects on the bottom surface of the wafer to look larger than identical objects on the top side of the wafer because light rays are bent at the silicone-sapphire interface. This magnification phenomenon is the same one that causes a fish in a pond to look larger than it actually is when looking down through the air-pond interface. In addition to this inherent lack of perfect microphotograph superposition, there are the normal problems in maintaining magnification ratios during enlarging and printing from one microphotograph to the next that also result in disregistry between microphotographs. Consequently, rather than trying to determine entrance-exit hole disregistry directly from superimposed photomicrographs, a least-mean-square fit of both the array of entrance holes and the array of exit holes to a straight line was carried out by digitizing the co-ordinates of the exit and entrance holes on the photomicrographs and following a standard least-mean-square fitting procedure. Once the best-fit straight lines were determined, the mean-square perpendicular deviations of the entrance- and exit-hole positions from the least-mean-square straight lines were calculated. For the entrance holes that were mechanically positioned on a straight line by the x-y table bed, this mean-square deviation was zero within the experimental error of $\pm 1.5\mu$. In contrast, on the exit side, the mean-square deviation of the exit holes from a straight line was significant ($\pm 12\mu$) as can be seen in Figures 2(b) and 3(b). Table I gives the average mean-square deviation of the exit holes from a least-mean-square straight-line fit for pulsed laser drilling at integrated power levels of 300 and 450 mW, respectively. A total of 40 drilled holes was measured at each power level. In the photomicrographs of Figures 2(b) and 3(b), the exit holes look elliptically elongated. This optical illusion occurs because the transparency of the SOS wafer on this polished interface allows one to see the slanted trail in the interior of the wafer. The resolved image of this slanted train plus the exit hole itself results in the elliptical shadow profile seen in Figures 2(b) and 3(b). The actual exit hole of the laser-drilled hole is located at the end of the ellipse that is in focus in the photomicrographs.

Table I. The average mean-square deviation (X^2) of the exit holes from a least-mean-squares straight-line fit for pulsed laser drilling through a 330-μ-thick silicon-on-sapphire wafer at integrated power levels of 300 and 450 mW. The entrance holes lay on a straight line with a zero mean-square deviation within experimental error.

(X^2)	Laser power level
$14.2 \pm 0.2 \times 10^{-7} cm^2$	300 mW
$11.7 \pm 0.2 \times 10^{-7} cm^2$	450 mW

3.1.2.2.2 Discussion

Pulse Separation. With the Q-switched frequency-doubled NdYAG laser[4] used in this investigation, the high-energy densities necessary for material removal and drilling are easy to attain. Although sapphire is essentially transparent at room temperature to the 0.532μ radiation used in this investigation,[4] some small amount of absorbtion raises the temperature of the Al_2O_3 to induce vaporization of the Al_2O_3[6]. The vaporized Al_2O_3 plasma absorbs the remainder of the energy in the Q-switched pulse and heats to a high pressure and temperature. Transfer of heat from the plasma to the sapphire heats the sapphire above the melting point. As the temperature rises even further, the high vapor pressure above the sapphire may temporarily suppress boiling. However, eventually the melted material will suddenly violently boil so that a mixture of vapor and liquid is ejected away from the beam impact point[6,7]. The resulting plume of gas and liquid must clear the drill hole before the next incoming pulse of the laser arrives[7]. Otherwise the plume will absorb all of the energy of the incoming pulse and further drilling will not occur. Thus, the separation time τ_p between laser pulses must exceed the time τ_c required for the exploding plume to clear the drill hole,

$$\tau_p > \tau_c. \qquad (1)$$

The maximum plume clearance time can be estimated from the frontal velocity V of the plume and the maximum drilling depth d,

$$\tau_c = d/V \qquad (2)$$

Plume ejection rates were measured by high-speed photography to be of the order of the speed of sound (3×10^4 cm/sec)[7]. Since the SOS wafers are 3.3×10^{-2} cm thick, the maximum plume clearance time is about 1μs. At the repetition rate of 1000 pulses psec used in the investigation, the pulse separation of 10^3 μsec clearly allows sufficient time for plume clearance between pulses in the absence of mode locking of the primary pulses.

Random Walk and Laser-Drilled Holes. Because of the large separation between the primary laser pulses relative to the plume clearance time, the drilling of a hole in a SOS wafer can be visualized as a series of independent material removal steps. As long as the material removed in each step is exactly below the material removed in the previous step, then the laser-drilled hole will proceed along a linear line in the sapphire crystal.

However, if the material removed by each laser pulse is not an exact spatial replica of the material removed by the previous laser pulse, the geometric center of the bottom of the drill hole will be slightly offset from the center of the drill hole tunnel just above it.

Consider a drill hole that has already experienced a net displacement X_{N-1} perpendicular to a straight-line path because of N - 1 previous laser pulses. The net displacement X_n after N pulses is then

$$X_n = N_{N-1} + S, \tag{3}$$

where S is the displacement perpendicular to a straight-line path caused by the Nth laser pulse. Squaring both sides of Equation (3) gives

$$X^2_N = X^2_{N-1} + 2X_{N-1} \cdot S + S^2 \tag{4}$$

If there is no correlation between the net displacement X_{N-1} after N - 1 laser pulses and the Nth displacement S, the term $X_{N-1} \cdot S$ will average to zero over many experiments. Thus, averaging of Equation (4) gives

$$(X^2_N) = (X^2_{N-1}) + (S^2) \tag{5}$$

Iterating Equation (5) (i.e., $(X^2_{N-1}) = (X^2_{N-2}) + (S^2)$: $(X^2_{N-2}) = (X^2_{N-3}) + (S^2)$; etc) gives

$$(X^2_N) = N(S^2), \tag{6}$$

where N is the number of times the pulsed laser beam has randomly displaced the bottom of the drill hole from an exact superpositioned path and (S^2) is the mean-square average of the variable size displacements of the bottom of the drill hole caused by each laser pulse.

The number of pulses used to form the drill hole through the SOS wafer can be calculated from the pulse frequency times the drilling times. For the 300 mW laser level, approximately 1000 pulses were needed to drill through 330 μ of sapphire. For the 450 mW power level, approximately 800 laser pulses were required.

Table II shows the measured mean-square displacement, the number of laser pulses that produced that displacement, the calculated average mean-square and average shift of the bottom of the laser hole per pulse, the average shift of the drill hole per pulse divided by the average diameter D of the drill hole, and the laser power level.

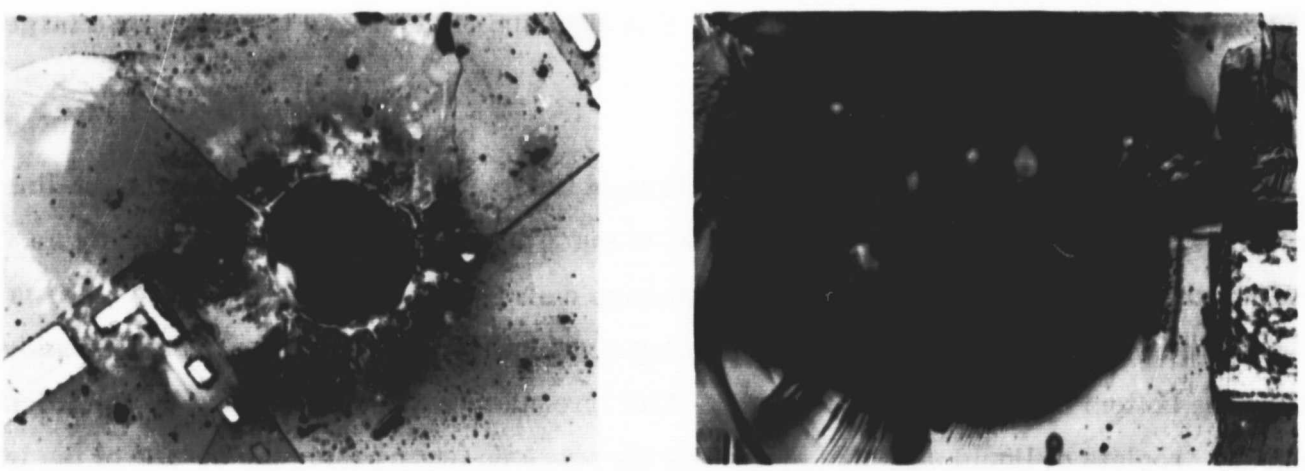
Table II. The observed average mean-square displacement of the exit position of the laser-drilled holes, the number N of laser pulses required to drill the holes through 330μ of sapphire, the calculated average mean-square and average shift of the bottom of the laser hole per laser pulse, the average shift divided by the average diameter D of the drill hole, and the integrated power level of the NdYAG laser.

(X^2)	N	(S^2)	$(S^2)^{1/2}$	$(S^2)^{1/2}/D$	Laser power level
14.2×10^{-7} cm^2	1000	14.2×10^{-10} cm^2	3.76×10^{-5} cm	4.7×10^{-2}	300 mW
11.7×10^{-7} cm^2	800	14.6×10^{-10} cm^2	3.82×10^{-5} cm	2.28×10^{-2}	450 mW

Several points are worth emphasizing in Table II. First, the actual displacement per laser pulse is small and is only a few percent of the hole diameter. Second, the displacement per laser pulse is approximately equal at both laser power levels. Hence, the random walk

displacement of the laser-drilled hole is lower at the higher laser energy level than at the lower level simply because fewer laser pulses are required to drill through the SOS wafer at the higher power level. If this line of reasoning is carried further, the conclusion is reached that a laser with a high enough power level to penetrate the SOS wafer in a single pulse should be used to drill the holes.

To test this idea, a few experiments were carried out with a high power NdYAG laser operating at 1.06μ, a pulse length of 0.5 msec, and a beam energy of 5 J. Holes could be drilled through the sapphire wafer with one pulse of this laser, and as expected, the displacements of the drilled holes were negligible compared to their diameters. Unfortunately, such a high-power pulse makes a large-diameter hole (106μ in diameter) which is on the large side for conductor feedthrough applications for integrated circuits. In addition, the high-power pulse caused spalling and cracking[8] of the sapphire wafer around the exit hole (Figure 4). Cracks extended 75μ into the interior of the 330μ-thick sapphire wafer and up to 300μ along the exit surface of the wafer. Such cracks and spalling are undesirable because they may cause breaks in the integrated circuits and lower process yields.



(a) (b)

Figure 4. (a) Circumferential and radial cracks around the exit position of a laser-drilled hole in a 330μ thick SOS wafer, that was made with one laser pulse. The linear and rectangular features in the photomicrograph are parts of an integrated circuit array on the SOS wafer (600X). (b) Severe spalling that occurred around the exit position of a laser drilled hole that was made with one laser pulse through a 330μ thick SOS wafer (600X).

A hole suitable for current feed-throughs for SOS wafers will require a laser with an integrated power level somewhere in between the limits that were tried in this investigation so that the number of pulses needed to drill through the wafer is about 30. With 30 pulses, hole random walk will be reduced to a negligible level and significant cracks and spalling of the wafer will be prevented.

Sources of Hole Displacements. There are several possible sources of the hole displacement, S, that occur during material removal with each laser pulse. The first such source is the spatial inhomogeneity[6] of the focused laser beam. Interference between indifferent modes in the solid-state laser cavity give rise to a very irregular intensity pattern in the focused spot, particularly at the high-output levels used for laser drilling. This irregular spatial profile of laser intensity changes from pulse to pulse[6]. Consequently, the laser beam intensity at the bottom of the drill hole will vary from point to point in an irregular and unpredictable manner. This variation in intensity will result in a nonuniform removal of material at the bottom of the drill hole that will change from one pulse to the next. Such nonuniform material removal contributes to a net displacement S of the drill hole from an otherwise straight-line trajectory. Displacements S caused by the irregular and changing irradiance patterns of the laser are in random directions such that the term $X_{N-1} \cdot S$ in Equation (4) averages to zero over a large number of pulses.

A second source of displacements S of the bottom of the laser drill hole from a straight-line trajectory is the internal multiple reflections[7] of the laser beam in the drill hole cavity as drilling progresses and the drill hole deviates from a straight-line course. Figure 5 shows a schematic diagram of a laser beam undergoing a number of total internal reflections before hitting the bottom of the laser-drilled hole. With irregular cavity walls caused by solidified splashed droplets of liquid sapphire ejected by the previous laser pulse, the course of the laser beam down the drill hole is random and unpredictable. If the light-piped laser beam does not hit the center of the cavity bottom as a result of the multiple internal reflections of the beam, then the cavity will be displaced from its straight-line trajectory. For example, in Figure 5, the cavity bottom will be displaced toward the right because the beam is striking the right-hand corner of the cavity. Because the impact point of the beam on the bottom of the cavity changes

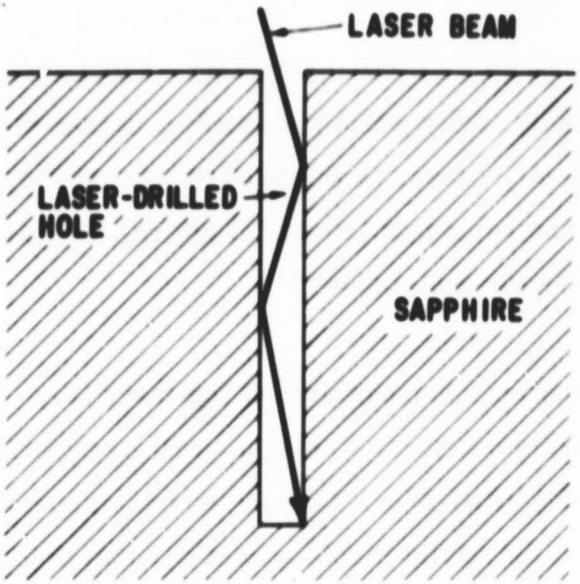


Figure 5. Multiple internal reflections of a laser beam in a laser-drilled hole result in the laser beam not striking the center of the bottom of the laser-drilled hole. In an actual laser-drilled cavity with irregular walls caused by splashing and solidification of ejected liquid sapphire, the laser beam path will vary randomly from one laser pulse to the next and cause random displacements of the bottom of the drill hole.

from one pulse to the next because of internal reflections from the changing irregular cavity walls, the term $X_{N-1} \cdot S$ in Equation (4) averages to zero over a large number of pulses.

Even before the drill hole deviates from a straight-line course, internal reflections may arise because the depth of focus is less than the drill-hole depth. (In this investigation, the depth of focus was 100μ and the drill-hole depth was 330 μ.) Past the focus point the diverging beam broadens out until it strikes the irregular walls of the drill hole. The resulting reflections around the periphery of the hole converge the beam back down the cavity until after perhaps several more reflections, the beam strikes the bottom of the drill hole in an essentially random position, resulting in a small random displacement of the bottom of the hole from its previous superimposed position.

The sources of hole displacements mentioned above are also present to some degree with a CW laser beam. For example, hole displacement arising from internal cavity reflections, caused by the depth of focus being less than the drill hole depth, will exist with both a

continuous and pulsed laser beam. On the other hand, random internal reflections in the drill-hole cavity caused by irregular cavity walls produced by splashed droplets of ejected sapphire are expected to be less with a CW laser beam that continuously vaporizes a material than with a pulsed laser beam where the bombarded material alternately goes through a violent solid to liquid to plasma transition during each pulse.

Finally, the change in the spatial inhomegenity[6] of the laser beam at the very high powers involved in pulsed operation from one pulse to another will be greater than the equivalent temporal change[9] in spatial inhomogeneity of a CW beam over the same drilling distance. Consequently, it is expected that the cavity displacement per unit drilling distance generated by changes in the spatial inhomogeneity of the laser beam will be greater with a laser operating in a pulsed mode than in a continuous mode.

A consideration of all three sources of hole displacements together produces a similar conclusion, namely that drill hole wandering will be greater with a laser operating in a pulsed mode than in a CW mode.

3.1.2.2.3 Summary

The exit positions of holes drilled through a Silicon-on-Sapphire wafer 330μ thick by a pulsed laser were found to have undergone a random-walk displacement from the hole entrance positions on the opposing face of the wafer. This random displacement increased with the number of laser pulses required to drill through the wafer. A model in which the bottom of the drill hole experiences small random displacements during each laser pulse because of beam intensity inhomogeneities and internal reflections in the drill was used to describe the experimental observations. The model indicates that the average random displacement caused by each laser pulse is only a few percent of the hole diameter. Such drill hole wandering can be reduced by using as few laser pulses as necessary to drill through the wafer, while at the same time avoiding the cracking spalling of the wafer that occurs with a hole drilled through the wafer with a single laser pulse.

3.1.2.3 Reverse Laser-Drilling of Sapphire

In order to form conductive feed-throughs in SOS, an array of holes were laser-drilled in each wafer for the purpose of permitting the implantation of a suitable conductor. During the development of techniques to laser drill holes in the SOS wafer, several unusual phenomena were observed. One such phenomenon, the random walk of the laser-drilled hole as drilling progressed from one side of the wafer to the other, was discussed in the previous section of this report. In this section, reverse laser drilling of SOS wafers is described. The process consists of hole drilling in which drilling proceeds upstream in the laser beam from the surface of the wafer where the laser beam exists towards the surface where the laser beam enters the wafer.

Sapphire wafers 5.08 cm in diameter and 0.033 cm thick with an orientation of (1102) $\pm$ 2 degrees were obtained from Union Carbide Crystal Products, San Diego, California. The front surface of the wafer has a polished optical finish while the real surface has a ground frosted appearance with a surface relief of $\pm$ 1 micron.

The laser drilling equipment used to reverse drill holes in the sapphire wafers was an Electro Scientific Industries Laser Trimming Systems Model 25 equipped with a NdYAG laser (1.06μ) with a 6.5 watt output in the CW mode. With the optics used in these experiments, the depth of focus was approximately 250 microns and the beam size was 75 microns in diameter. For reverse drilling, the laser was operated in a repetitively Q-switched mode. As illustrated schematically in Figure 6, during the drilling sequence, the laser emitted a continuous train of individual pulses at a pulse repetition rate of 3 kHz and a pulse duration of 200 nanoseconds for a period of 5 msec. This initial train of pulses was followed by a delay time of 45 msec and then a second train of pulses identical to the first pulse train. The sequence was repeated over and over again until the drill hole was through the wafer. The 3 kHz pulse repetition rate was selected because it gives the highest output power of the laser operating in the repetitively Q-switched mode. Each pulse train was led by a giant pulse as shown in Figure 6. This giant pulse is important because it greatly increases the absorption coefficient of the layer where drilling initiates, allowing the following smaller pulses to vaporize and drill the sapphire[11]. A series of separate pulse trains was used rather than one continuous pulse train in order to obtain more of the desirable giant pulses. The delay time of 45 msec between pulse trains was

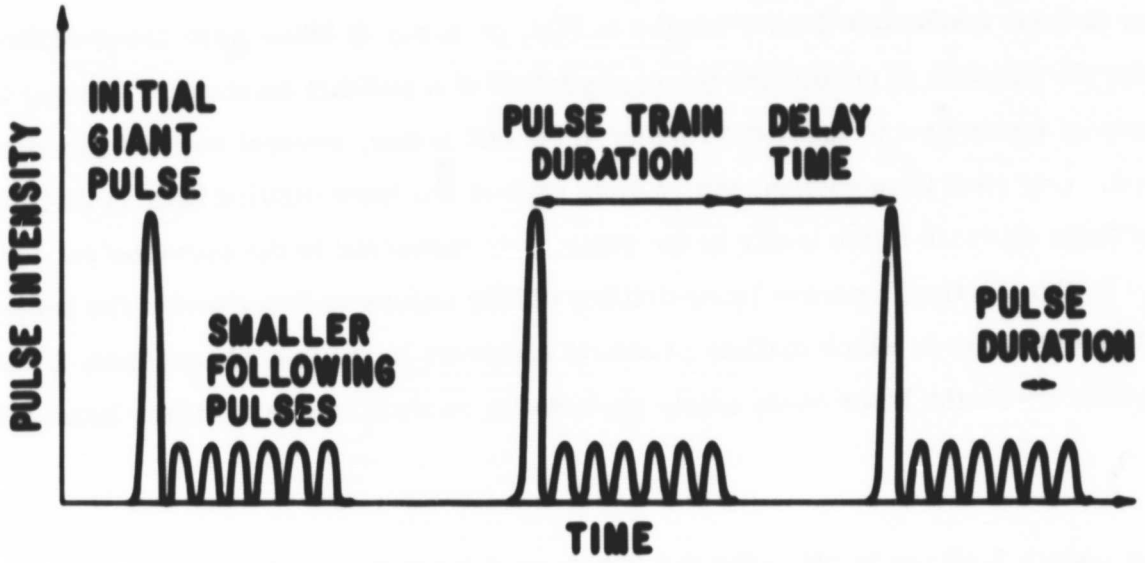


Figure 6. The laser beam intensity versus time for a laser operated in a repetitively Q-switched mode with time delays between successive pulse trains.

selected so that the flash lamps would have sufficient time to pump up the NdYAG crystal to an energy density where a giant pulse would be produced on initiation of a repetitive Q-switching train of pulses. (The number of pulse trains used for drilling was varied from 1 to 75 trains.) During different drilling experiments, the wafer was placed in three different positions. In the first series of experiments, the wafer rested on a polycrystalline alumina substrate 625 microns thick. In the second series of experiments, the wafer was positioned 625 microns above the polycrystalline alumina substrate. Finally, in the last series of experiments, the wafer was suspended in free space. The position of the wafer with respect to the focal point of the laser was kept constant in the three different positions and was chosen to maximize drilling yield. Separate drilling experiments were tried with the laser beam incident on the polished and on the ground surfaces, respectively, of the sapphire wafer in the three different positions.

3.1.2.3.1 Experimental Results

Reverse laser drilling was an unexpected discovery made in the course of this experiment. It was found that under certain conditions laser drilling initiated on the wafer surface where the laser beam exited rather than on the wafer surface where the laser beam entered the wafer.

Following initiation of drilling on the exit surface, laser drilling then progressed upstream in the laser beam towards the entrance beam surface as shown schematically in Figure 7. Figure 8 shows a photomicrograph of a sapphire wafer submerged in water and positioned at a 45 degree angle to the optic axis of the microscope to allow one to observe a sequence of drill holes in the wafer. A series of partially laser-drilled holes were formed in the wafer with 1, 3, 5, 7 and 9 laser pulse trains, respectively, with the laser beam entering the wafer from above as depicted for the first hole. The polished entrance surface of the wafer is invisible in the photomicrograph. A dotted line, therefore, has been drawn on the photomicrograph to show the position of the entrance surface of the wafer. The rear exit surface of the wafer is visible because of its ground, rough surface topology. The number of laser pulse trains used to drill each hole is shown below each hole. From the photomicrograph, it can be seen that laser drilling initiated on the wafer surface where the laser beam was exiting and progressed toward the wafer surface where the laser beam entered the wafer. Nine laser pulse trains were required to drill a hole completely through the wafer.

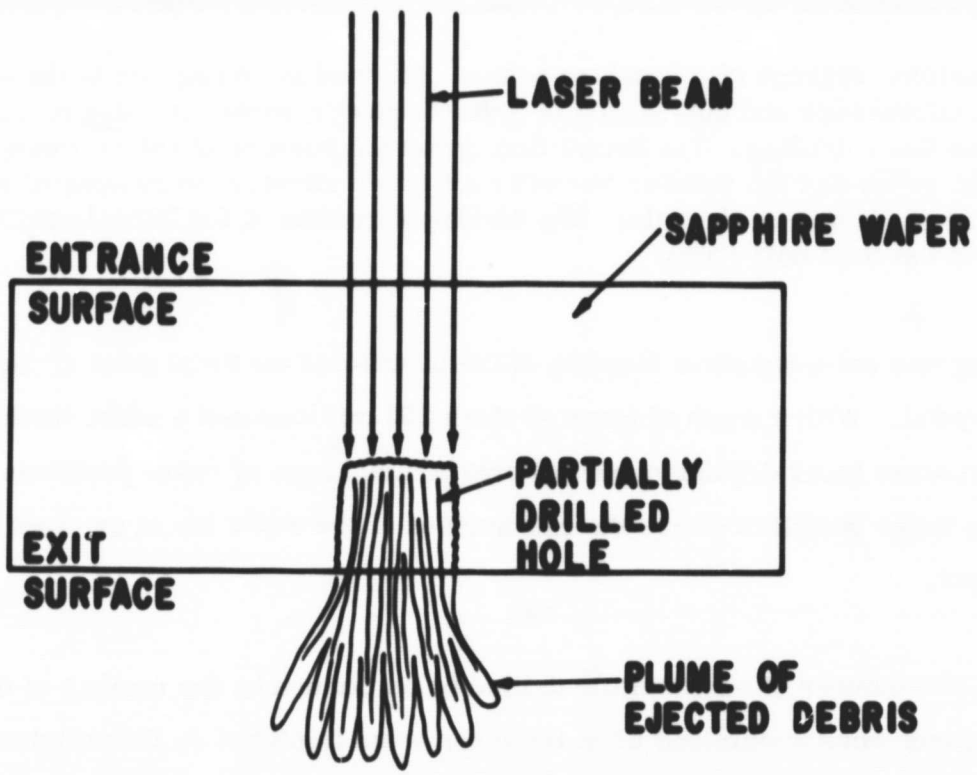


Figure 7. The reverse laser drilling of a sapphire wafer. Drilling initiates on the wafer surface where the laser beam exits and proceeds upstream towards the wafer surface where the laser beam enters.

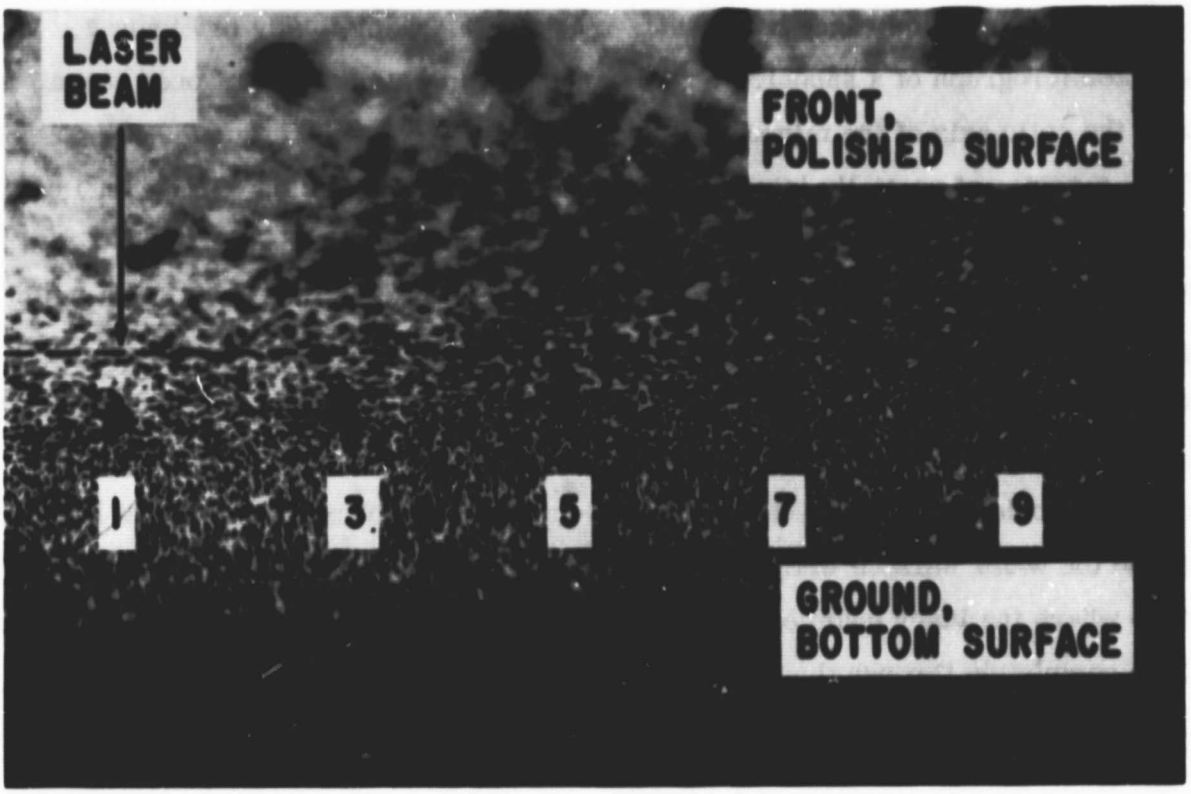


Figure 8. A photomicrograph of a sapphire wafer positioned at 45 degrees to the optic axis of a microscope and submerged in water to show a series of holes formed by reverse laser drilling. The dotted line shows the position of the entrance surface of the water and the number beneath each hole indicates the number of laser pulse trains used to form the hole. The incident direction of the laser beam is shown above the first hole (70X).

Reverse drilling was not a sensitive function of the position of the focal point of the laser in the sapphire crystal. With a depth of focus of about 250 microns and a wafer thickness of 325 microns, reverse laser drilling occurred over a wide range of wafer positions and was not limited to those wafer positions where the exit surface of the wafer lay in or close to the focal plane of the laser.

Drilling yields (the number of successfully drilled holes divided by the number of drill hole positions attempted) were maximized when the laser beam impinged on the polished surface of the wafer. A 50% decrease in yields occurred when the laser beam impinged on the ground surface of the wafer.

Laser drilling was very sensitive to local surface conditions. Figure 9 shows a photomicrograph of an evenly spaced row of attempted drill holes in a sapphire wafer with each hole position being bombarded by 30 laser pulse trains. All but one hole position yielded holes that extended all the way through the wafer. In contrast, the unsuccessful drilled hole position does not even show any evidence of initiation of drilling. It was found that one could return again and again to such positions (the machine positioner was accurate to $\pm$ 1 micron) and try drilling and not be successful.

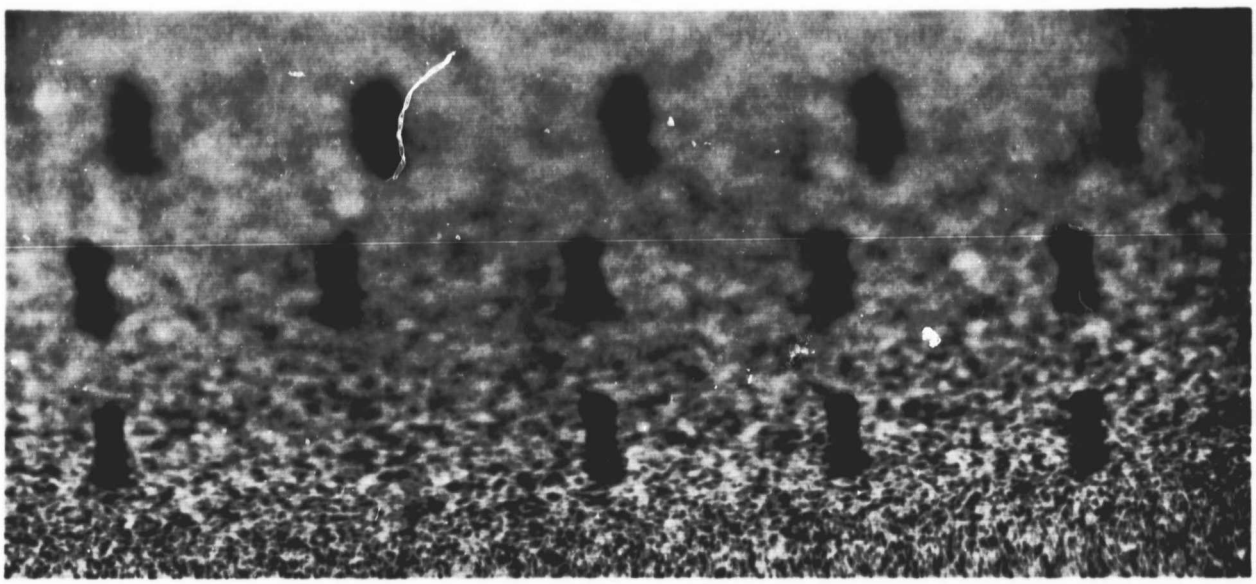


Figure 9. Effect of local surface conditions on drilling. A photomicrograph similar to Figure 3 of an evenly spaced row of attempted drill holes in a sapphire wafer with each hole position being subjected to 30 laser pulse trains. All positions except one yielded drill holes completely through the wafer. The unsuccessful position does not even show any evidence of initiation of drilling (70X).

Drilling yields also varied from one wafer lot to another. In particular, it was found that reverse laser drilling was more difficult on wafers that were 7.62 cm in diameter than wafers that were 5.08 cm in diameter although both wafer lots were obtained from the same source.

Drilling yields were maximized (100%) when the sapphire wafer was placed on a polycrystalline alumina backup disk. Unfortunately, the relected debris from laser drilling (see Figure 7) had

no place to go to in this situation so that the drill holes became encrusted and plugged near the exit surface of the wafer by recondensed debris. When the sapphire wafer was suspended in space with no material behind it, drilling yields dropped to about 90% although the holes were clean and unencumbered with recondensed debris. A good compromise between these two situations was achieved when the alumina backup disk was placed 625 microns from the rear exit surface of the sapphire wafer. Drilling yields ranging from 95 to 100%, depending on the wafer lot, were achieved in this case with unclogged and relatively clean drill holes.

3.1.2.3.2 Discussion

Reverse Laser Drilling. There are several possible explanations of the reverse laser drilling observed in this investigation. Reverse laser drilling could be simply a focal plane positioning phenomenon. That is, when the focal plane of the laser beam is located at or near the exit surface of the sapphire wafer, drilling initiates there. However, several facts suggest that focal plane position is not the cause of reverse laser drilling. First of all, reverse laser drilling was not observed in an earlier investigation when a higher intensity laser beam was being used[10]. Secondly, reverse laser drilling occurred over a relatively wide range of wafer positions parallel to the laser beam and was not a sensitive function of wafer position as would be the case if focal point positioning were critical. Finally, the depth of focus of the laser beam was comparable to the wafer thickness so it would be difficult to position the wafer so that only the exit surface was lying in the focal region of the beam.

Another possible cause of reverse laser drilling is a moving laser-beam focal spot caused by self-trapping and self-focussing of the laser beam arising from the nonlinearity of the index of refraction of sapphire in high electric fields [12-14]. In this case, the damage track initiates at the point of highest intensity in the material (focal plane) and propagates upstream towards the laser source and reaches its maximum length when the incident laser pulse intensity reaches its peak [14]. A number of differences between the reverse laser drilling observed in this investigation and laser beam self-trapping indicate that self-trapping is not the cause of reverse laser drilling. First of all, self-trapping is a single pulse phenomenon with the entire upstream propagation of the damage track occurring within the duration of a single pulse. As can be seen in Figure 8, the reverse drilling required multiple pulse trains and therefore many individual

pulses. Secondly, the damage track in self-trapping is physically different than the drill hole observed in reverse drilling. With self-trapping, the damage track has a filamentary character with a long (500 microns) and narrow (2-10 microns) profile with beads of larger areas of damage spread out along the filament [14]. The reverse laser-drilled holes shown in Figures 8 and 9 are very different in character.

The most probable cause of reverse laser drilling is the destructive and constructive interferences between the primary and reflected laser beams that occur, respectively, on the entrance and exit surfaces of the sapphire wafer as shown schematically in Figure 10. On the entrance surface, the reflected beam experiences a phase change of π on reflection because the beam is passing from a lower to a higher index of refraction medium. The resulting destructive interference reduces the laser beam intensity at the entrance surface of 52% of the impinging intensity of the beam. The beam transmitted through the entrance surface also has only 52% of the impinging beam intensity. Consequently, on or near the entrance surface the laser beam is weakened by the effects of reflection.

In contrast on the exit face of the sapphire wafer, constructive interference increases the transmitted laser beam intensity from 52% to 85% of the beam intensity incident on the wafer. Constructive interference occurs on the exit face of the wafer because light reflecting from a surface where a light beam is passing from a higher to a lower index of refraction medium suffers no phase change. In other words, when light strikes a boundary from the side of lower velocity, no phase change happens, whereas when light strikes a boundary from the side of higher velocity, a phase change of π occurs. This phenomenon is the same type encountered in the reflection of simple mechanical waves, such as sound waves in solids or a transverse wave in a rope. Reflection with a change in phase where the velocity decreases in crossing the boundary (entrance surface) corresponds to the reflection of waves from the fixed end of a rope. Here the elastic reaction of the fixed end of the rope immediately produces a reflected train of opposite phase traveling back along the rope. The case where the velocity increases in crossing the boundary (exit surface) has its parallel in reflection from a free end of a rope. The end of the rope undergoes a displacement twice the amount it would if the wave were continuous (constructive interference) and it immediately starts a wave in the reverse direction having the same phase as the incident wave.

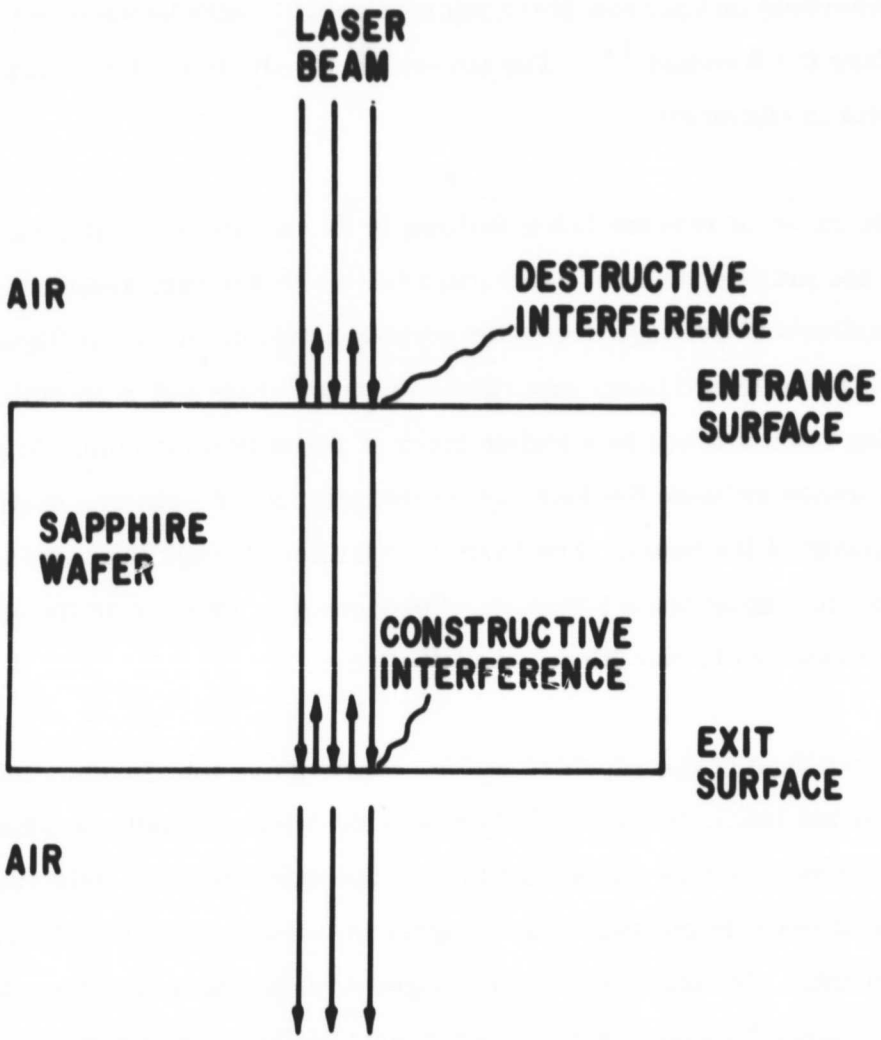


Figure 10. A laser beam passing through a sapphire wafer in air destructively interferes with its reflected component on the entrance surface of the wafer because of a phase change of π that the reflected beam experiences at an air-to-sapphire interface and constructively interferes with its internally reflected component on the exit surface of the wafer because the internally reflected beam experiences no phase change at the sapphire-to-air interface.

It is clear if intensity of the original laser beam is very high, drilling will initiate on the entrance surface as was observed in other investigations [10, 11, 12, 13] since destructive interference with the reflected beam is not enough to reduce a high beam intensity below the intrinsic damage threshold for sapphire. Thus, relatively high intensity laser beams will result in forward laser drilling of sapphire.

Moreover, if the intensity of the original laser beam is too low, the constructive interference on the exit face of the wafer will not boost the beam intensity enough to initiate drilling there. Hence, low intensity laser beams will not laser drill sapphire.

Consequently, only a window exists in the available range of laser beam intensities that is compatible with reverse laser drilling. A first-order calculation of this intensity range can be made as follows. With reference to Figure 11, a laser beam with an electric field strength, E_o, is shown impinging on a sapphire wafer. A reflected beam with a strength r E_o is reflected from the entrance surface of wafer with a phase change of π. Here r is the amplitude coefficient of reflection for the air-sapphire interface. A transmitted beam of strength $E_o(1-r)$ leaves the entrance surface, passes through the sapphire wafer and strikes the exit surface of the wafer. A beam of intensity r $E_o(1-r)$ is reflected from the exit surface with no phase change, while a beam of strength $E_o(1-r)^2$ is transmitted through the exit surface.

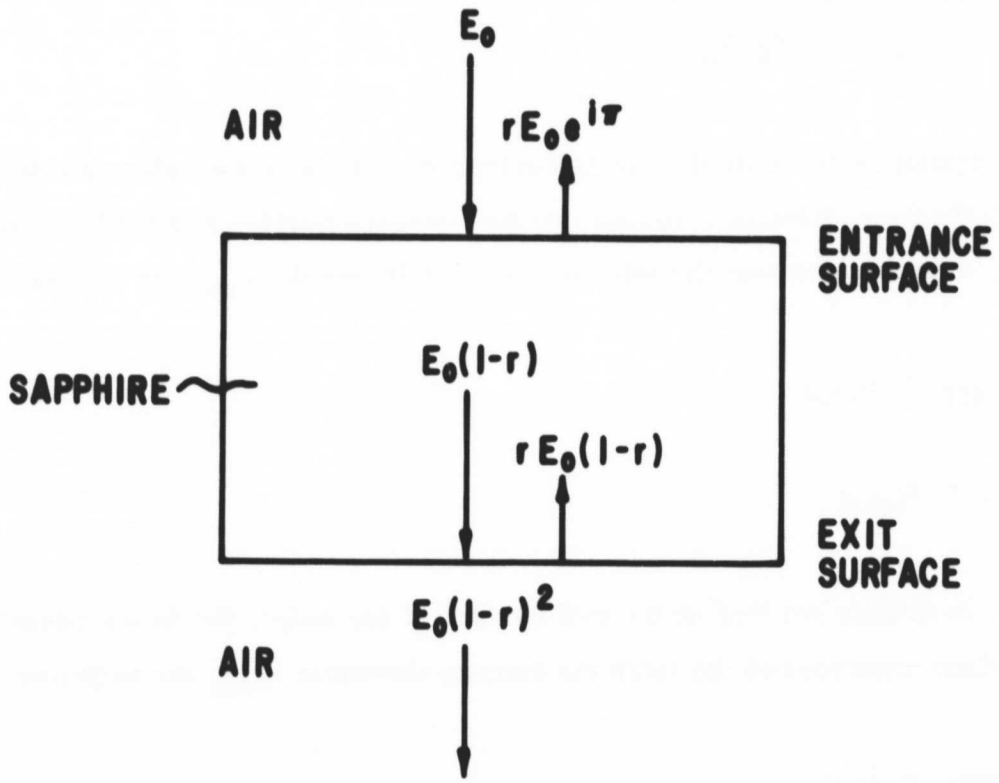


Figure 11. A schematic diagram of a laser beam impinging on a sapphire wafer with an electric field strength E_o. r is the amplitude coefficient of reflection for sapphire. The reflected beam from the entrance surface experiences a phase change of π while the reflected beam from the exit surface does not change phase.

The intensity of the laser beam on the entrance surface, I_{ENTR}, is given by

$$I_{ENTR} = |E_o + r\,E_o e^{i\pi}|^2 = E_o^2\,(1-r)^2 \tag{1}$$

The intensity of the transmitted beam in the wafer I_{IN}, is

$$I_{IN} = E_o^2\,(1-r)^2 \tag{2}$$

Similarly, the intensity of the beam on the exit surface of the wafer, I_{EXIT} is,

$$I_{EXIT} = |E_o(1-r) + rE_o(1-r)|^2 = (1+r)^2 E_o^2 (1-r)^2 \tag{3}$$

To avoid initiation of laser drilling on the entrance surface of the wafer or internally in the wafer, both the beam intensity, I_{ENTR}, on the entrance surface and the beam intensity of the wafer, I_{IN}, must be less than the intrinsic damage threshold I_{DAM} for sapphire

$$I_{EXIT} < I_{DAM}$$
$$I_{IN} < I_{DAM} \tag{4}$$

In contrast, to initiate drilling on the exit surface of the wafer, the beam intensity I_{EXIT} at the exit surface must exceed the intrinsic damage threshold I_{DAM} for sapphire

$$I_{EXIT} > I_{DAM} \tag{5}$$

The combination of equations 1 - 5 give the incident beam intensity, $I_o = E_o^2$, range over which reverse laser drilling occurs.

$$\frac{1}{(1+r)^2(1-r)^2} < \frac{I_o}{I_{DAM}} < \frac{1}{(1-r)^2} \tag{6}$$

The amplitude coefficient of reflection is given by

$$r = \frac{n-1}{n+1} \tag{7}$$

where n is the index of refraction of the material being drilled. From Equations (6) and (7), the conditions for the reverse laser drilling of various transparent materials can be determined. Figure 12 is a laser drilling map for transparent media showing the ranges of incident laser beam intensity normalized by the intrinsic damage threshold intensity of a material versus the index of refraction of a material. Above curve B, forward laser drilling will occur. Between curves B and A, conditions are favorable for reverse laser drilling. Below curve A, no drilling will occur.

One possible question about the first order model presented above is why construction interference between the reflected beam from the exit surface and the transmitted beam in the interior of the wafer does not initiate damage in the interior of the wafer as well as on the exit surface. Two factors offer an explanation for this. First, it is probably easier to nucleate damage on the surface as compared to the interior of the wafer because the surface represents a discontinuity where atomic bonding is weakened. Secondly, the roughened nature of the rear exit surface of a Silicon-on-Sapphire wafer causes some random scattering and spreading of the reflected laser beam so that the effect of constructive interference is a maximum at the rear surface.

Drilling Yields. Drilling yields (the number of successfully drilled holes divided by the number of drill holes attempted) were highest when the laser beam impinged on the polished surface rather than the ground surface of the sapphire wafer for reverse laser drilling. The reason

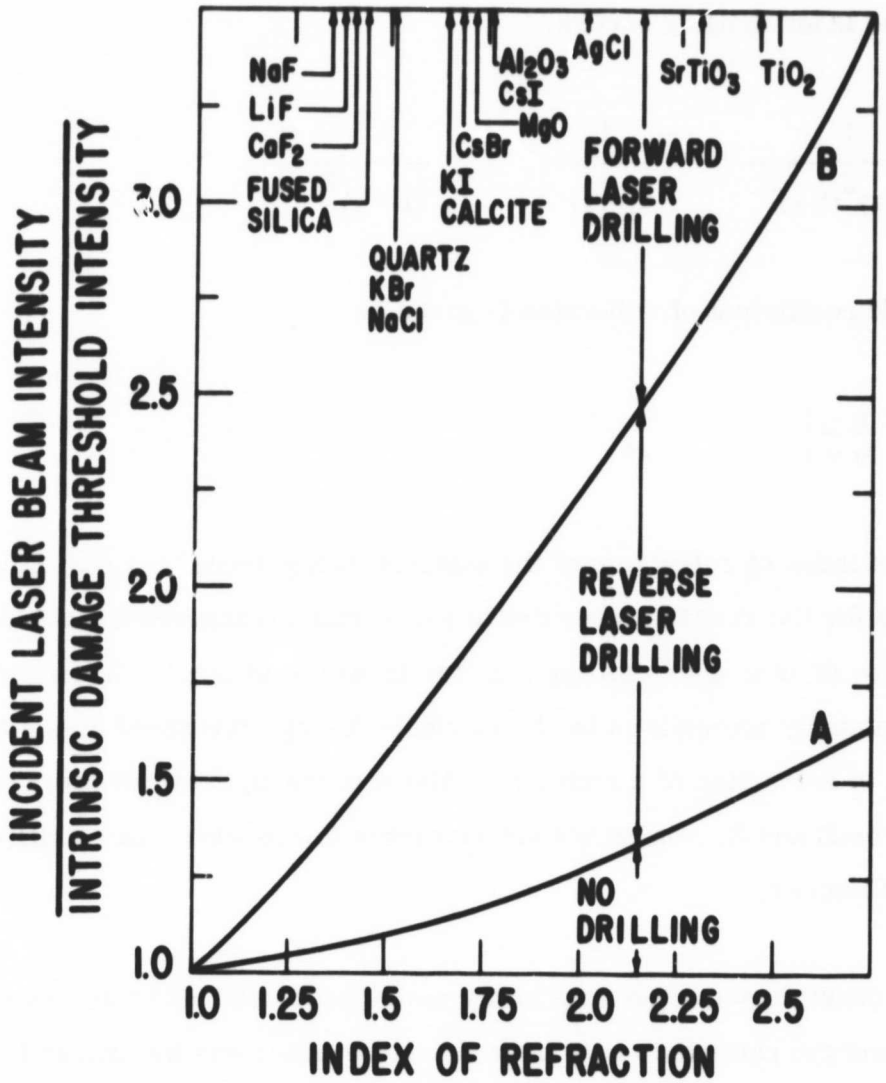


Figure 12. A laser drilling map for transparent materials showing the different types of drilling regions whose boundaries are functions of the index of refraction of the material and the incident laser beam intensity. Above curve B, only forward laser drilling will occur. Between curves B and A, conditions are favorable for reverse laser drilling. Below curve A, no drilling will take place.

for this difference is illustrated schematically in Figures 13(a) and 13(b). When the laser beam is incident on the polished surface of the wafer (Figure 13(a), the beam remains tightly bunched until it strikes the ground exit surface of the wafer. The tightly bunched beam has a intensity that favors initiation of reverse drilling on the exit face, thus maximizing drilling yields.

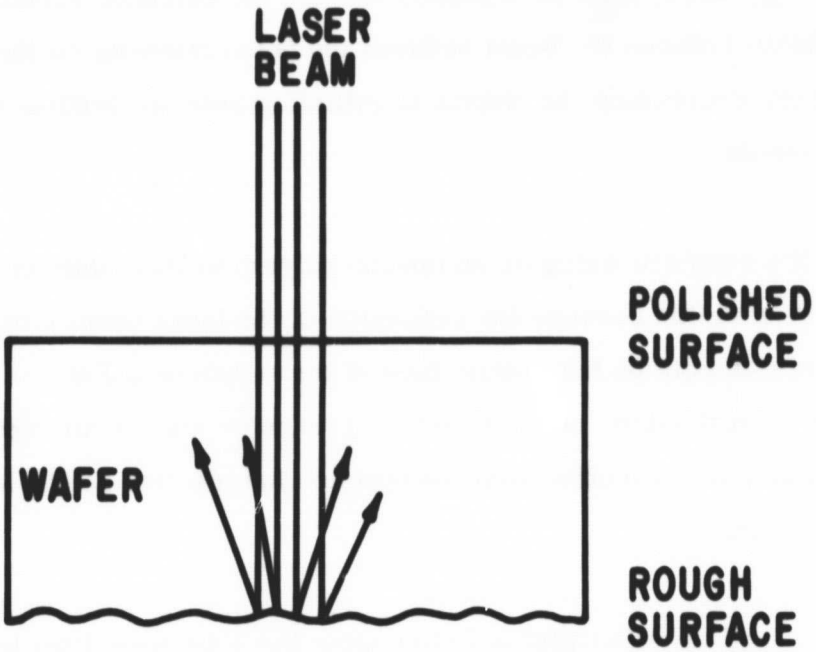


Figure 13(a). **A laser beam incident on the polished face of a Silicon-on Sapphire wafer remains tightly bunched until it hits the exit face of the wafer, thereby maximizing reverse laser drilling yields.**

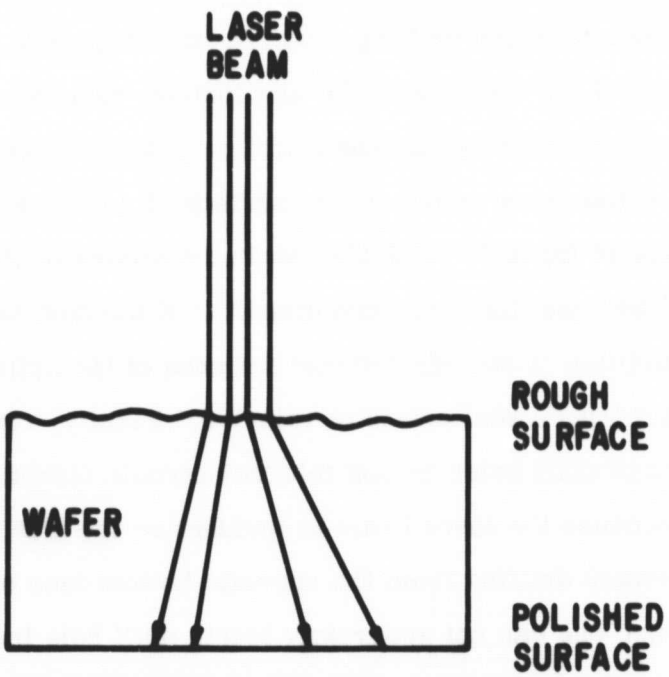


Figure 13(b). **A laser beam incident on the rough ground face of a Silicon-on-Saphire wafer is scattered and spread as it passes through the surface, thereby decreasing the beam intensity on the exit surface of the wafer and thus reducing reverse laser drilling yields.**

In contrast, when the laser beam impinges on the rough surface of the wafer (Figure 13(b)) the beam tends to diverge and spread as it passes through the entrance surface of the wafer. The spreading of the beam reduces the beam reduces the beam intensity on the polished exit face of the wafer, thereby decreasing the chance of initiating reverse drilling on the exit face, thus reducing drilling yields.

The placement of the sapphire wafer on an opaque polycrystalline alumina backup disk increased reverse laser drilling yields because the reflection of the laser beam from the alumina disk increased the beam intensity on the bottom face of the sapphire wafer. In addition to increasing the beam intensity by reflection, some direct heat transfer may occur between the sapphire wafer and the plasma plume ejected from the opaque alumina disk as the disk is drilled by the transmitted laser beam.

Advantages of Reverse Laser Drilling in Fabricating the Massively Parallel Processor. Reverse laser drilling has three advantages over forward laser drilling when fabricating holes in Silicon-on-Sapphire wafers for feed-through conductors for the massively parallel processor. First, reverse laser drilling minimizes the amount of debris that is deposited on the front device surface of the wafer during laser drilling. As shown in Figure 7, all of the debris is ejected out of the rear face of the wafer until the last instant, thereby minimizing any possible damage to electronic circuits on the top polished surface of the SOS wafer. Secondly, reverse laser drilling saves real estate area on the device surface of an SOS wafer. Laser drilled holes have a certain degree of taper [16] with the maximum diameter of the hole being on the initiation side of the drill hole and the minimum diameter of the hole being on the exit side of the drill hole. Reverse drilling is so oriented that the area of the drill hole is minimized on the device side of the wafer where real estate is valuable. Finally, reverse laser drilling allows accurate placement of drill holes among microelectronic circuits on the device side of commercial SOS wafers because the laser beam is incident on the side where the electronic circuits are located. Forward drilling from the opposite bottom face of commercial SOS wafers is not practical since one can not accurately locate drill hole locations with respect to microelectronic circuits on the top wafer surface through the foggy ground bottom surface of SOS wafers.

SECTION 4

CONDUCTOR IMPLANTATION IN DRILLED HOLES IN SAPPHIRE

SECTION 4

CONDUCTOR IMPLANTATION IN DRILLED HOLES IN SAPPHIRE

To form conductive feed-through in Silicon-on-Sapphire (SOS), six techniques were used to implant conductors in laser-drilled holes in SOS wafers. These will be examined and compared in this section. The implantation techniques include capillary wetting, wedge extrusion, wire insertion, electroless plating, electroforming, and double-sided sputtering with through-hole electroplating.

A 10 x 10 array of holes on 250 micron centers was laser drilled through SOS wafers with an Electro Scientific Industries Laser Trimming Systems Model 25 equipped with a NdYAG laser (1.06 μ) with a 6.5 watt output in the CW mode[17]. The laser was operated in a repetitively Q-switched mode. A 5 msec train of individual pulses at a pulse rate of 3 kHz and an individual pulse duration of 200 nanoseconds was emitted by the laser every 45 msec until the drill hole was through the sapphire wafer. Approximately nine such laser pulse trains were required to drill a hole completely through the wafer. Drilling was done in the reverse laser drilling mode where laser drilling initiates on the surface of the sapphire wafer where the laser beam exits and proceeds upstream in the laser beam to the surface where the laser beam enters the wafer[17]. The wafer was oriented so the laser beam impinged on the front polished surface and exited through the ground rear surface of the wafer. The laser-drilled holes were, on the average, 57 microns in diameter and were 330 microns long. For the sake of comparison, larger holes were also drilled in the wafers by overlapping individual drill holes. These larger holes had diameters of 80, 100, 125 and 150 microns, respectively.

4.1 IMPLANTATION BY CAPILLARY WETTING

One means of implanting a conductor in the laser-drilled holes in the sapphire wafer is to paint the backside of the wafer with a conductor-filled liquid that wets sapphire. Because the liquid wets sapphire, it is drawn by capillary action into the laser-drilled holes, carrying the suspended conducting particles with it (Figure 14). Once the holes are filled, the liquid can be cured to form the implanted conductor. Two such conductor-filled liquids were obtained from commercial vendors for evaluation. The first was an epoxy-based liquid called Ablebond 826-1, manufactured by Ablestik Laboratories in Gardena, California. This epoxy is a one-

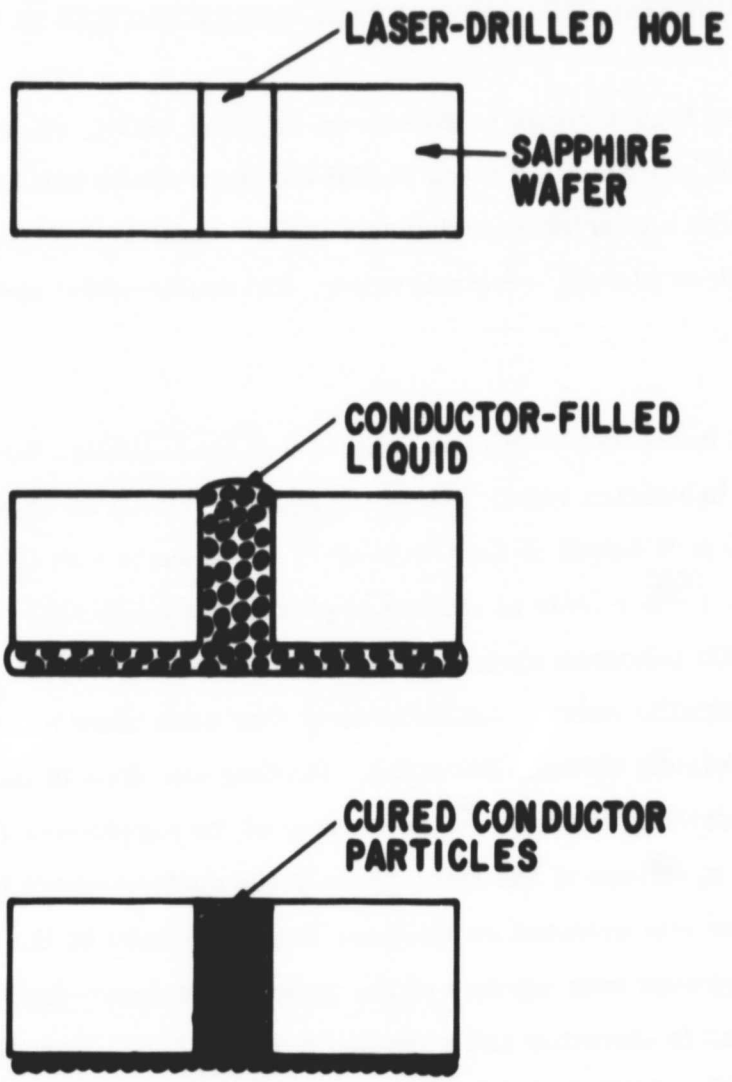


Figure 14. Implantation of a feedthrough conductor in a laser-drilled hole in an SOS wafer by capillary wetting and curing of a conductor-filled liquid.

component, 100% solids, pure silver-filled conductive epoxy that has a volume resistivity of 10^{-4} ohm-cm after curing for one-half hour at 150°C. The second conductive liquid was a silicone-polyimide liquid with a designation of BE-225H made by Bergston and Associates in Summit, New Jersey. This polyimide is a two-component, 80% solids, pure silver-filled conductive polyimide that also has a volume resistivity of 10^{-4} ohm-cm after curing by solvent evaporation for two hours at 150°C. Both liquids wet sapphire and thus are ideally suited for implantation by capillary wetting. The advantage of the epoxy-based liquid is that there is no

discernible shrinkage on curing. In contrast, as the solvent evaporates during curing of the polimide-based liquid, it shrinks about 20%. The advantages of the silicone polyimide are that it will withstand high temperatures (550°C for one-half hour in pure oxygen) and that it exhibits no outgassing once it is cured. Both liquids contained rough angular silver particles with an average diameter of approximately 4 microns.

Because the laser-drilled holes are very small, and because the conductor-filled liquids were viscous, an estimate of the time required to fill a hole by capillary wetting was made to see if the hole sizes, hole lengths and liquid viscosities were compatible with a reasonable fill time.

Equation 4.1 is the Hagen-Poiseuille Law for the flow of liquid in a cylindrical tube[18]

$$Q = \frac{\pi \Delta P D^4}{128 \mu h} \tag{4.1}$$

where Q is the volume flow rate, ΔP is the static pressure difference over a tube length of h, D is the diameter of the tube, and μ is the viscosity of the liquid.

For a liquid being drawn in a tube by capillary action, the pressure difference in the liquid between the entrance of the tube and the meniscus of the liquid in the tube is

$$\Delta P = \frac{2 \gamma}{D} \tag{4.2}$$

where γ is the surface tension of the liquid.

The volume flow rate in the tube is also given by:

$$Q = \frac{\pi D^2}{4} \frac{dh}{dt} \tag{4.3}$$

where h is the distance the liquid has moved into the tube. Combining Equations (4.1), (4.2), and (4.3) and integrating:

$$\int_0^{\tau} dt = \frac{16\mu}{D\gamma} \int_0^{H} hdh$$

$$\tau = \frac{8\mu H^2}{D\gamma} \qquad (4.4)$$

where τ is the time required to fill a tube of length H by capillary wetting. For the laser-drilled holes in the sapphire wafers, H = 3.3×10^{-2} cm, D = 5.7×10^{-3} cm. Both the epoxy and silicon polyimide liquids had similar viscosities and surface energies which were estimated to be: γ = 50 dynes/cm and μ = 25 poise. Substituting these values in Equation (4.4) gives a reasonable fill time τ of 0.76 seconds.

Fill times of this order were observed for the four different hole sizes, which ranged between 57 and 150 microns in diameter, that were tried in this investigation. The composition of the liquid in the laser-drilled hole, however, varied greatly with hole size. For the holes that were 125 and 150 microns in diameter, the composition of the liquid implanted in the holes was that of the initial conductor-filled liquid. In contrast, for the smaller laser-drilled holes that were 100, 80 and 57 microns in diameter, the concentration of silver particles in the liquid in the hole dropped rapidly with decreasing hole size. In fact, the smallest hole size contained essentially no silver particles and was filled with only the pure carrier liquid as shown in Figure 15. Microscopic observation indicated that the four-micron silver particles became clup clumped together and formed a log jam at the hole entrance. This log jam of particles prevented the movement of particles into the hole while allowing the infiltration of the pure carrier liquid. Several means of forcing the silver particles into the holes were tried. First, a vacuum was produced on one face of the wafer so the ambient pressure on the opposite face of the wafer would force the liquid suspension into the hole. This only caused pure liquid to flow through and exude from the hole, while the silver particles remained clumped and jammed near the hole entrance. Next, the wafer was subjected to ultrasonic vibrations both with and without the use of vacuum to see if the vibrations would break up the log jam of particles at the hole entrance. This technique also failed to implant the silver particles in the hole.

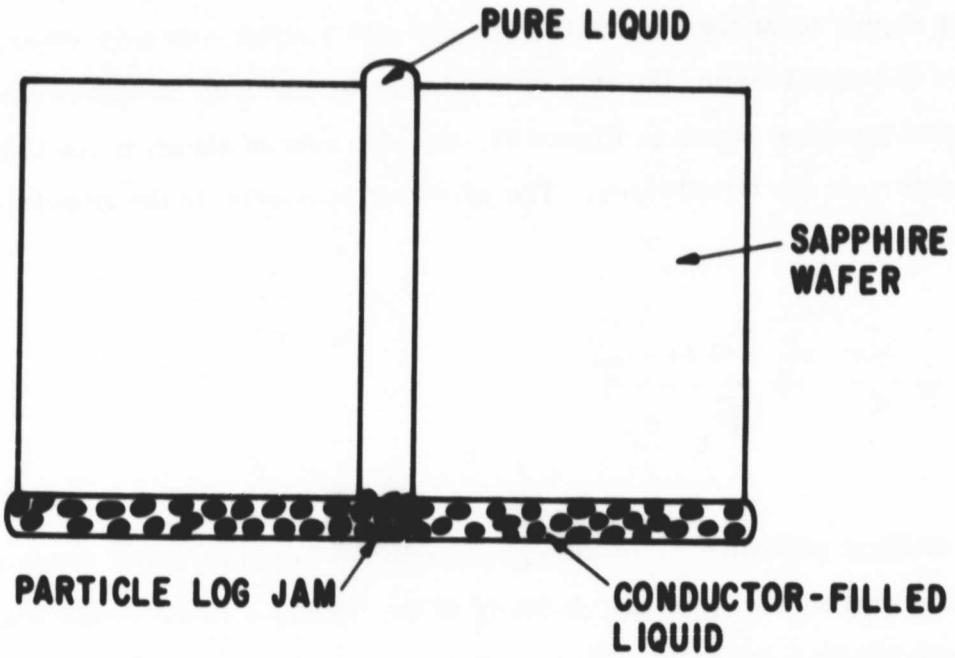


Figure 15. A log jam of conductor particles at entrance to a laser-drilled hole prevents the particles from flowing into the hole along with the carrier liquid.

If, then, the 100-micron hole size is taken as the cutoff hole size below which log jamming of the four-micron silver particles becomes significant, then implantation by capillary wetting is probably not feasible below a hole-size/particle-diameter ratio of approximately 25. An analysis of this flow problem is very difficult. To date, analyses have been only tired for very dilute suspensions in tubes[19] and not for highly concentrated suspensions such as were used in this investigation.

4.2 IMPLANTATION BY WEDGE EXTRUSION

Equation (4.4) shows that the filling time of a laser-drilled hole by capillary wetting increases linearly with the viscosity of the wetting suspension. For very viscous conductor-filled suspensions, the filling time can become unreasonably long. Consequently, any technique in which the viscosity of the suspension does not change the filling time might prove to be valuable. Such a technique is wedge extrusion of a viscous suspension of conductor particles into the laser-

drilled holes. It is well known that two solid bodies can easily slide over one another when a thin layer of liquid between them has a high positive pressure. As shown in Figure 16, to develop a high positive pressure in a liquid layer between the two planar solid bodies, the planes of the respective bodies must form a small angle and move relative to each other. As a result of the thinness of the liquid layer, the rate of strain due to viscosity is high in the liquid. With the wedge-like configuration shown in Figure 16, the high rate of strain in the liquid layer produces a high pressure in the liquid layer. The pressure developed in the liquid layer is given by[20]:

$$P - P_o = \frac{6\mu U}{\alpha} \frac{(d_1 - d)(d - d_2)}{d^2 (d_1 + d_2)} \tag{4.5}$$

where P_o is the ambient pressure, P is the pressure in the liquid layer, U is the relative velocity of the two solid bodies, μ is the viscosity of the liquid, α is the wedge angle, d is the separation distance between the solid bodies, and d_1 is the maximum and d_2 is the minimum distance between the solid bodies. From Equation (4.5), when $d_1 > d_2$, the pressure P is positive and varies throughout the layer with a single maximum.

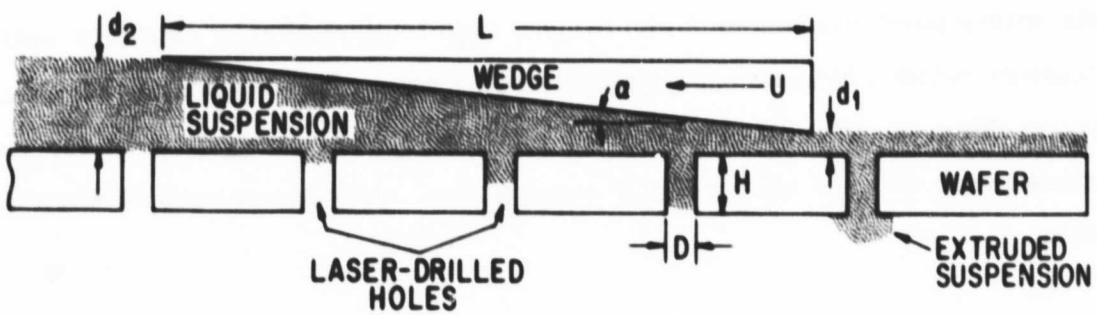


Figure 16. A cross section of a moving wedge (upper body) separated by a layer of liquid suspension from a wafer (lower body) with an array of laser-drilled holes. The positive pressure generated in the liquid layer by the moving wedge extrudes the viscous liquid suspension into the laser-drilled holes. The ability to extrude the liquid into the holes is surprisingly independent of the viscosity of the liquid, the length of the wedge, and the velocity of the wedge.

The positive pressure developed in the liquid layer can be used to extrude the liquid in the layer into cavities in one of the solid bodies. For example, if the lower body in Figure 16 is an SOS wafer with an array of laser-drilled holes and the fluid is a suspension of conductor particles, then moving the top wedge body with respect to the SOS wafer will force the liquid suspension in the laser-drilled holes in the wafer, thereby implanting the conductor fluid. From Equations (4.1) and (4.3), the rate of flow of liquid in a laser-drilled hole is given by

$$\frac{dh}{dt} = \frac{\Delta P\, D^2}{32\, \mu\, h} \tag{4.6}$$

With the upper wedge body moving at a constant velocity U over the SOS wafer, the extrusion pressure ΔP will change with time, since the separation distance d between a particular laser-drilled hole and the sliding overhead wedge will change with the position of the wedge. For any particular laser-drilled hole, the separation d between it and the overhead wedge varies as

$$d = d_2 + (d_1 - d_2)\, \frac{U}{L} t, \quad 0 < t < \frac{L}{U} \tag{4.7}$$

where U is the velocity of the overhead body and L is its length. From Equations (4.5) and (4.7), the pressure causing extrusion into the laser-drilled holes, consequently,

$$\Delta P(t) = \frac{6\mu U}{\alpha}\, \frac{(d_1 - d_2 - \beta t)\, (\beta t)}{(d_2 + \beta t)^2\, (d_1 + d_2)} \tag{4.8}$$

where

$$\beta = (d_1 - d_2)\, \frac{U}{L}$$

Combining Equations (4.6) and (4.8) and integrating the hole length from zero to H and the time from zero to U/L yields

$$H^2 = \frac{3 D^2 L}{8 (d_2^2 - d_1^2) \alpha} \left[L - (d_1 + d_2) \mid n \frac{L}{d_2} \right] \qquad (4.9)$$

In the usual case when $L >> d_1$, d_2 and $d_2 >> d_1$ and thus $d_2/L \approx \alpha$, Equation (4.9), ignoring a numerical factor of $(3/8)^{1/2} = 0.6$ reduces to

$$H = D \alpha^{-3/2} \qquad (4.10)$$

Equation (4.10) states, in words, that for a given diameter D and length H of a laser-drilled hole, the ability to fill the hole by wedge extrusion depends only on the angle α that the wedge makes with the SOS wafer. Filling is independent of the viscosity of the liquid suspension, the velocity of the wedge, and the length of the wedge. For laser-drilled holes with a diameter of 57 microns in a SOS wafer that is 330 microns thick, the wedge angle α must be less than 0.3 radians in order for the wedge extrusion action to completely fill the holes.

The same two conductor-filled liquids that were used with implantation by capillary wetting were used again for the wedge extrusion experiments. A wedge of engineering plastic was moved at a wedge angle of 0.1 radians over a sapphire wafer with a thin layer of conductor-filled liquid on its surface. For holes greater in diameter than 100 microns, the wedge extrusion method filled the laser-drilled holes with the liquid suspension. For the laser-drilled holes with diameters less than or equal to 100 microns, a log jam of silver particles occurred at the entrance of the laser-drilled holes and prevented the silver particles from entering into the hole, although the pure carrier liquid was extruded into the hole. The results were similar to those found in the capillary-wetting implantation method. Since wedge extrusion is independent of the viscosity of a liquid suspension, the failure of the silver particles to move into the laser-drilled holes in both cases is most likely caused by a mechanical interlocking of the irregular silver particles as flow is constricted near the entrance of the laser-drilled hole, and is not due to an abnormally high viscosity of the liquid suspension.

4.3 IMPLANTATION BY WIRE INSERTION AND ELECTROPLATING

The third method of implanting conducting feed-throughs in the laser-drilled holes in SOS wafers was wire insertion and electroplating. Tungsten wires 13 microns in diameter were guided into the laser-drilled holes from a glass capillary tube while observing with a 20X biocular microscope. The glass capillary tube prevented the end of the thin tungsten wire from vibrating and thus facilitated wire insertion into the holes. An array of tungsten wires was threaded through a stack of laser-drilled SOS wafers. Each wafer had an identical array of laser-drilled holes. The tunsgten wires were temporarily bundled together, and the wafer-wire complex was placed in a copper electroplating solution, and copper was electroplated onto the wires until the wires were 75 microns in diameter (Figure 17). The electroplated copper serves two purposes: first, it locks the wire firmly in the laser-drilled hole; secondly, it considerably stiffens the wires so that on removal from the electroplating solution, the wafer-wire array is a mechanically rigid structure.

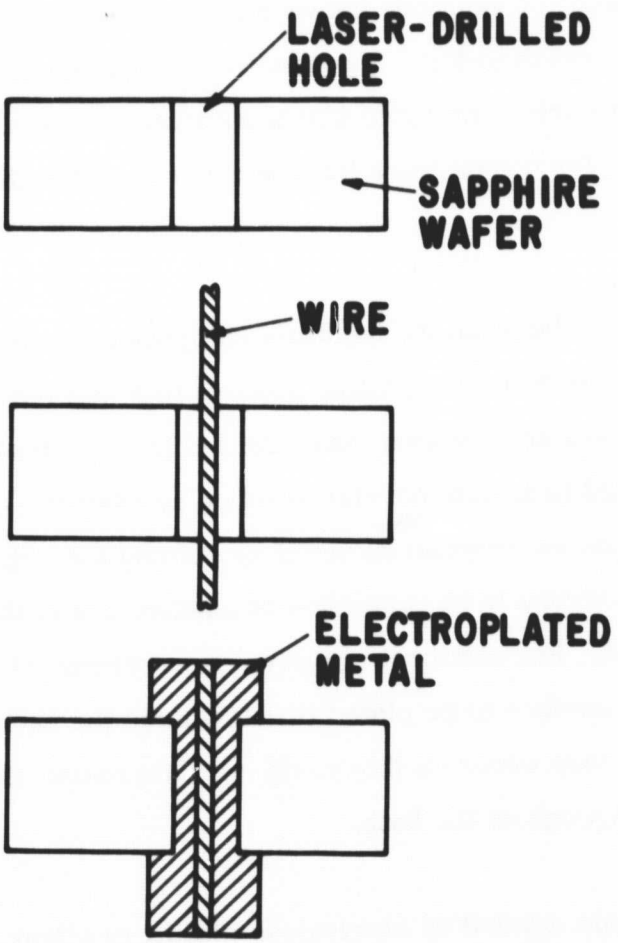


Figure 17. Implantation of a feedthrough conductor in a laser-drilled hole in SOS by wire insertion and electroplating.

Insertion of a seed wire and electroplating is a straightforward, dependable means of forming feed-through conductors when the number of feedthroughs required is small (less than a thousand). With a larger number of holes, insertion and keeping track of the wires in array becomes tedious, thereby making this method impracticable.

4.4 IMPLANTATION BY ELECTROLESS PLATING

Printed circuit boards typically have circuit patterns on both sides of the plastic laminate board to save space. In order to make electrical connections between the two sides of the board, holes are drilled or punched through the board and a suitable conductor is implanted in the hole. Of the three ways of doing this, by eyelets, jumpers, or "plated-through holes," the "plated-through holes" method has won general acceptance.

In this process, a plastic laminate coated with copper foil on both surfaces has holes drilled or punched through where connections between the two sides are required. The holes as formed are nonconductive, and therefore, a conductive coating must be applied to the plastic surfaces of the holes. Of various methods that were tried, chemical reduction plating was found to be the most suitable for depositing a thin, conductive and stable film of uniform thickness in a hole[9, 10].

Because of the similarity between the feedthrough problem for SOS wafers and for printed circuit boards, the chemical reduction plating process that was commercially successful with printed circuit boards was tried with a laser-drilled holes in SOS. In chemical reduction plating, usually referred to in commercial practice as electroless plating, a metal ion in solution is reduced to the corresponding metal by gaining the required number of electrons. The source of these electrons is the oxidation of another ion in the solution which is referred to as the reducing agent. For the most effective use of chemical reduction baths, a catalyst must be present on the surface to be plated that localizes the chemical reduction so that electroless plating will only occur on this surface. Otherwise, the metal ions in solution would be precipitated throughout the bath.

The metal most commonly applied by electroless plating is silver, by the well-known Brashears process that was used in the past for silvering mirrors. However, because of limitations due

to the migration of silver in electrical circuits, copper was selected instead for electroless plating in the laser-drilled holes in SOS.

If an electroless plating solution is tc be useful in depositing more than a thin flash of metal, the metal being deposited must itself by a catalyst for further reduction, since the original catalyst on the surface is rapidly buried. Because copper is only an effective catalyst in an electroless plating bath using a Fehling-formaldehyde solution[22], all of the work in this investigation was done using this solution.

Commercial preparations of this solution were obtained from MacDermid, Inc. of Waterbury, Conn. and Shipley Co. of Newton, Mass. The electroless plating is essentially a three-stage process: first, a clean SOS wafer with laser-drilled holes is dipped into an aqueous solution containing a dissolved catalyst ($PdCl_3$). Next, the wafer is dipped into an activator solution containing a reducing agent that causes Pd to precipitate out on all surfaces of the SOS wafer, including those in the laser-drilled holes. Finally, a modified Fehling-formaldehyde solution is passed through the laser-drilled holes. This solution contains both dissolved copper ions and a reducing agent. Reduction is at first catalysed by the Pd atoms on the walls of the laser-drilled hole, and they by the deposited copper atoms themselves as electroless plating proceeds and covers up the Pd atoms.

The results of electroless plating of the laser-drilled holes were encouraging. Copper was deposited in the 75 micron diameter holes, and an electrical connection between the two faces of the wafer with a resistance of about 10^{-2} ohms per hole was made. In general, however, the electroless plating was uneven and erratic. Some areas plated well, while other areas did not plate at all. Consequently, the problem of implantation yield could be serious with this technique. The erratic electroless plating behavior on sapphire seems to be associated with the sapphire surface, since plastic breakers used in the experiments plated evenly. Apparently, etchants that are applied as part of the commercial process create an extensive network of deep interlocking channels inside, and fine shallow pits on the surface of plastic. This network serves both as a place where the Pd catalyst can rest without getting washed away and a topographical mechanical lock to ensure good adhesion of the diposited copper to the plastic substrate[23]. Such a network is absent in the case of sapphire, because it is highly resistant

to most etches. The lack of such network is probably the root cause of the erratic electroless plating of copper on SOS.

4.5 IMPLANTATION BY ELECTROFORMING

A fifth method of implanting feedthrough conductors in laser-drilled holes in SOS is by electroforming. As shown in Figure 18, a hole is first drilled in an SOS wafer. Next, a metal film is deposited on the back face of the SOS wafer to serve as the cathode in the subsequent electroforming process. The wafer is then placed parallel to a copper anode in a copper electroplating solution (Figure 19) and a dc current is passed between the copper anode and the metal film cathode on the wafer. It was found that copper ion currents preferentially deposited copper around the edges of the laser-drilled hole on the rear face of the SOS wafer because of the enhanced electrical field caused by the sharp radius of curvature here. These copper deposites quickly sealed the hole over and a plug of copper, fed by copper ion currents through the laser-drilled hole, grew towards the front face of the wafer (Figures 18 and 19). On reaching the front surface of the wafer, a semispherical cap of copper grew on top of the plug at a rate much faster than the growth rate of the plug in the hole because of the greater availability of copper ions at the front surface of the wafer.

In order to form a uniform plug that completely filled the hole and that did not form dendritic branches with entrapped pockets of plating solution, a special electroplating solution with organic additives had to be used. This electroplating solution was an aqueous solution of 250 grams per liter of $CuSO_4 \cdot 5H_2O$, 15 grams per liter of H_2SO_4, 0.01 gram per liter of N_2H_4CS, and 0.8 gram per liter of molasses[24]. With 75 micron diameter holes, a nominal dc current of one milliamp per hole was applied for 1.5 hours to electroform the copper implants. The anode to cathode spacing was one cm. During electroforming, most of the applied current did not actually go down the holes to form the implants, but went around to the rear face of the wafer. The actual current density in the laser-drilled holes was about 160 mA/cm^2. At higher current densities, dendrite formation and branching of the plugs occurred, resulting in spongy type plugs with occluded pockets of electroplating solution.

Several problems were encountered with electroforming feedthroughs: first, a number of holes would contain air bubbles that would block or inhibit the electroforming process after submerging

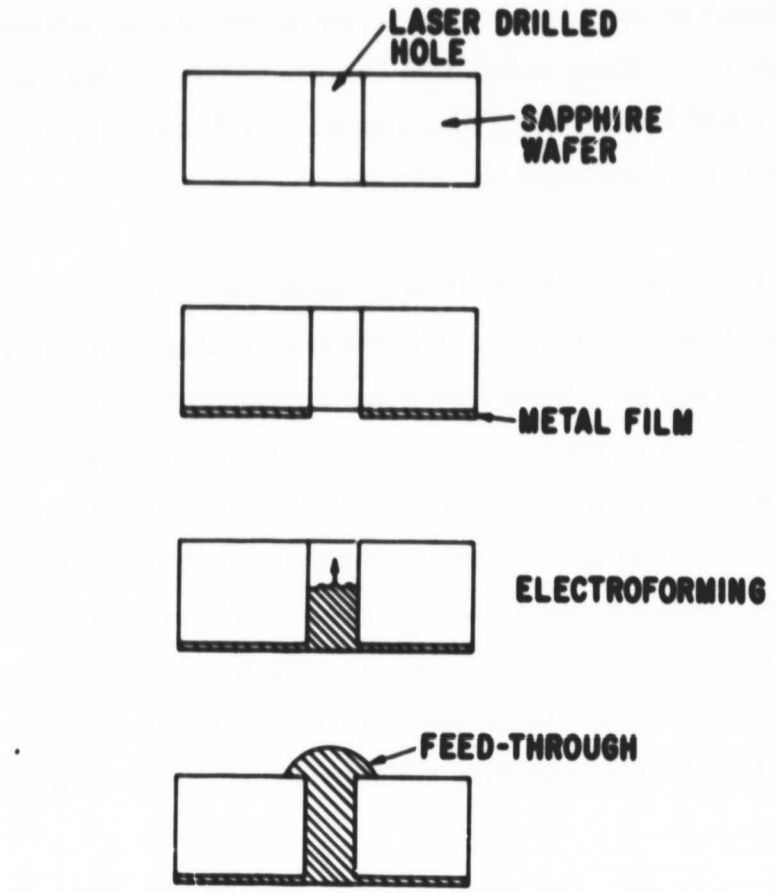


Figure 18. The steps involved in the implantation of a feedthrough conductor in a laser-drilled hole in SOS by electroforming.

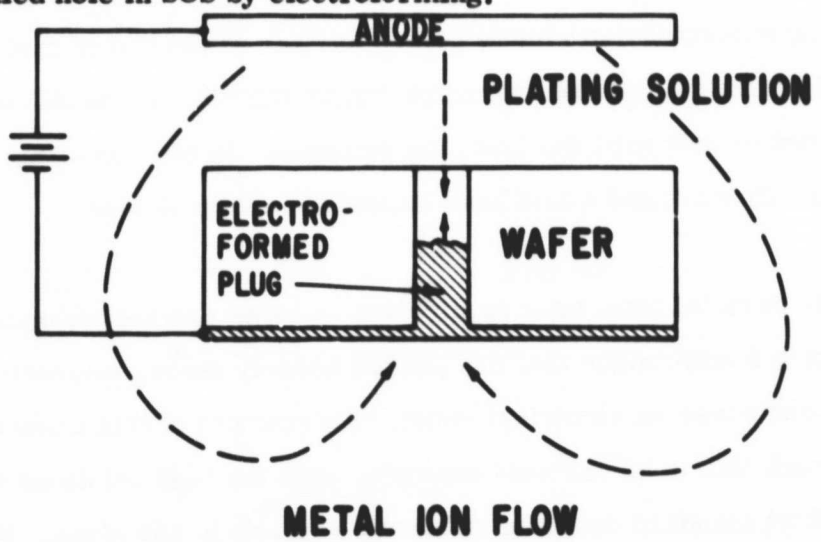


Figure 19. Electroforming a feedthrough in SOS. The preferential deposition of metal around the edges of the laser-drilled hole on the rear face of the wafer sealed over the hole and led to the subsequent growth of the metal plug through the hole towards the front surface.

the SOS wafer in the electroplating bath. This air bubble problem was eliminated by predipping the wafers in methanol before placing them in the electroplating solution. Methanol which wets sapphire was drawn by capillary action into the laser-drilled holes, thereby expelling all of the air bubbles. The small amount of methanol in the holes diffused away on subsequent submergence of the wafer in the electroplating solution.

A second problem that arose in electroforming feedthroughs in SOS arose from the uneven growth rate of plugs in different holes. Electroforming plugs in holes is an unstable process, since the closer the plug grows toward the front surface where copper ions are readily available, the faster the plug will grow. Thus, if two plugs begin at the same position, a random fluctuation that causes one plug to grow a little faster than its neighbor will be magnified by the instability of the process into an ever-growing difference in their growth rates and lengths. The actual problem is not as bad as the ideal case presented here, because organic additives in the solution will preferentially polarize and slow the growth rate of a fast-growing plug with its associated high current density. By trying solutions of different compositions and concentrations, it was found that the electroplating solution described above minimized the uneven growth rate problem.

Unfortunately, even small differences in growth rates of the plugs were greatly magnified as the plugs emerged at the front surface of the wafer and the fast-growing spherical caps began to form. One plug emerging one minute before another at the end of a 90-minute electroforming process would form a spherical cap much larger than its neighbor. In order to obtain a 100% yield, one had to wait until the last plug emerged. In the meantime, the spherical caps of those plugs already emerged would have expanded rapidly in size.

For the massively parallel processor application, a large and variable cap size is undesirable because neighboring feedthroughs that are packed densely among microelectronic circuits could touch each other and cause an electrical short. An example of this uneven cap size is shown in Figure 20. Although this is an extreme example, with the best solutions and best plating conditions, the smallest standard deviation achieved was 10% in cap sizes. With only several thousand holes, such a standard deviation is acceptable, since only a few standard deviations with this number of holes need be considered. However, with one million holes, the cap size

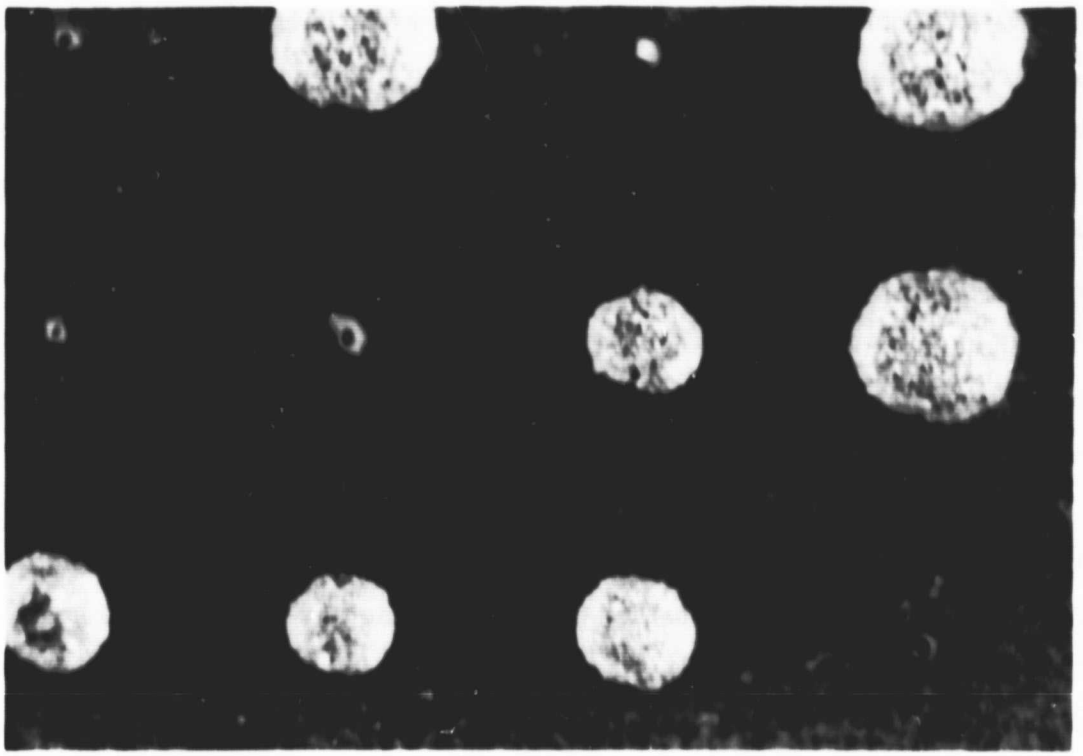


Figure 20. Variable semispherical cap sizes on electroformed plugs in SOS caused by a small difference in emergence times of individual plugs at the front surface of the wafer during electroforming (32X)

sould only be specified within a six standard deviation range (i.e., $\pm$ 60%) with any certainty. This difference in cap sizes is too large to be acceptable for the massively parallel processor application. Consequently, there was a need to further reduce the difference in spherical cap sizes. This was done by periodic reverse platting. Figure 21(a) shows a graph of the electroplating current versus time and a schematic diagram of a wafer with electroformed implants growing in laser-drilled holes. By periodically reversing the electroplating current, plug dissolution and plug growth occur for times of τ_D and τ_p, respectively. If growth of the electroformed plugs in the laser-drilled holes is diffusion limited, then plugs nearer the surface have a diffusion relaxation time less than the diffusion relaxation time of plugs further from the surface. This difference in diffusion relaxation times can be taken advantage of by having the time period of the dissolution cycle τ_D be greater than and less than, respectively, the diffusion relaxation times of plugs near and far away from the surface. With this situation, plugs at a distance L less than $\sqrt{D_s \tau_D}$ will be preferentially dissolved, while those plugs at a distance L

greater than $D_s\tau_D$ will be relatively immune to dissolution during the dissolving cycle. (D_s is the diffusion coefficient in the solution.) If the time-current integrals of the plating and dissolution cycles are made equal, then the plugs will all tend to even out at the same distance below the surface of the wafer. By controlling the length of the dissolution cycle τ_D, the level below the surface at which this occurs can also be controlled. A typical electroforming process with periodic reverse plating is as follows: first, the plugs are grown free with simple dc current until they approach the front surface. Then, periodic reverse plating is applied to even out the plug lengths and the dissolution cycle time τ_D is gradually reduced to bring the plugs right up to the front surface where a short plate cycle grows small, semispherical caps with a good size uniformity.

For example, an actual leveling of a 10 x 10 array on 100 mil centers of copper implants at a distance of 12 microns from the front surface of a 2 in. diameter SOS wafer was accomplished with an applied plating current of 100 mA, an applied dissolution current of 1000 mA, a plating cycle time of 5 sec, and a dissolution cycle time of 0.2 sec. Because an indeterminable portion of the plating and the dissolution current sink on the rear face of the wafer, the actual time-current integrals that produce leveling have to be found experimentally. Figure 21b shows an array of electroformed feedthroughs processed with reverse periodic plating. A comparison with Figure 20 indicates the improvement in size uniformity.

4.6 IMPLANTATION BY DOUBLE-SIDED SPUTTERING AND THROUGH-HOLE AND ELECTROPLATING

A final method of successfully implating feedthrough conductors in laser-drilled holes in SOS is by double-sided sputtering and through-hole electroplating. As shown in Figure 22, after forming a hole 75 microns in diameter through the 330-micron thick SOS wafer by laser drilling, a one-micron thick metal film is sputtered deposited on both faces of the wafer. Enough metal is deposited on the sidewalls of the laser-drilled hole during sputtering to make an electrical contact with a resistance of 30,000 ohms per hole between the opposing faces of the wafer. This resistance is too high to be useful, so that through-hole electroplating is necessary to reduce the resistance.

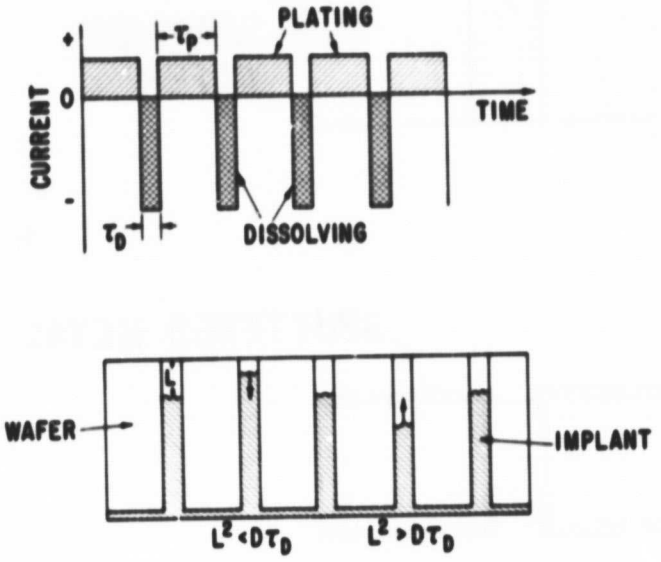


Figure 21(a). Leveling of implants by periodic reverse plating. Implants close to the surface are preferentially dissolved during the reverse plating pulse.

Figure 21(b). Semispherical cap sizes on feedthrough plugs in SOS electroformed with periodic reverse plating (25X)

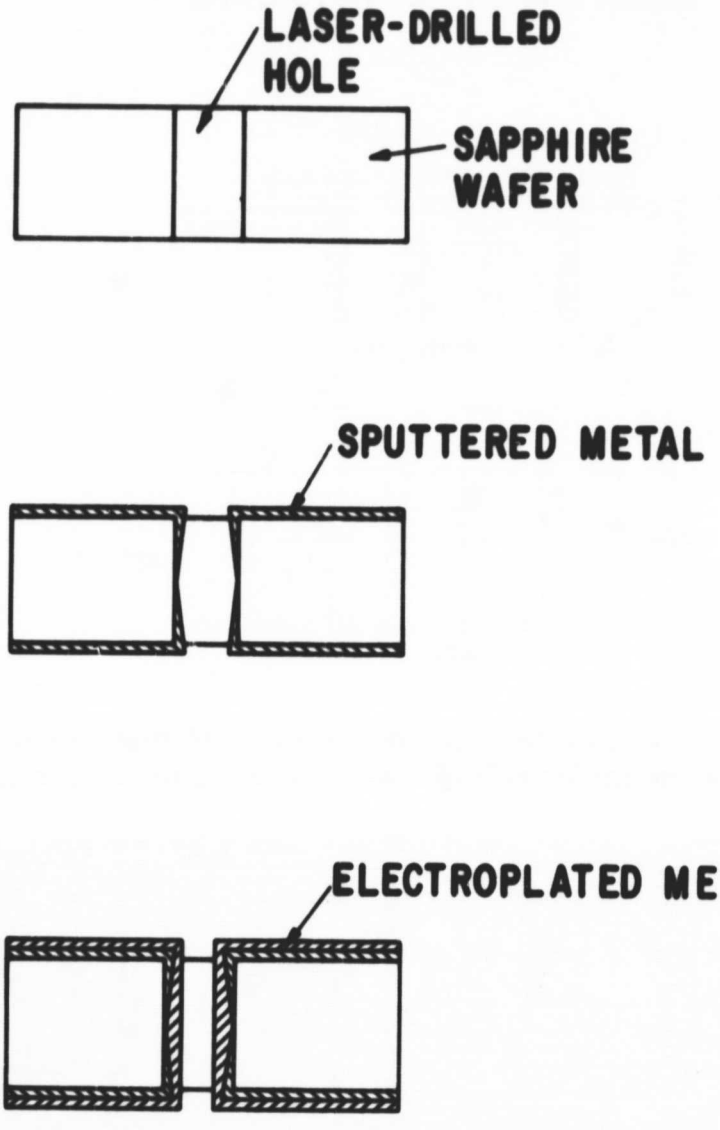


Figure 22. Implantation of a hollow feedthrough in a SOS wafer by double-sided sputtering and through-hole electroplating.

Because of the high electrical fields associated with the sharp radius of curvature of the wafer surface at the exit and entrance edges of a laser-drilled hole, the rate of electrodeposition is very high here, causing the ends of the hole to become plugged during electroplating. Plugging of the holes is undesirable because of the possibility of leaving entrapped electroplating solution in the hole, and because a hollow implant is useful later when individual wafers must be electrically interconnected in a stacked array. The solution to the problem of the hole plugging has its roots in the interesting mathematical similarity between the equations which describe

the electrical field and the equations which describe the fluid velocity around the end corners of the laser-drilled hole. If ϕ_E is the voltage potential around the end corners of the hole, then the electrical field E associated with this potential is derivable from this potential:

$$E_i = \frac{\partial \phi_E}{\partial X_i} \tag{4.11}$$

If irrotational field flow is assumed for simplicity around the end corners of the hole, then the fluid velocity U is also derivable from a potential ψ_U[20], which is a stream function of ϕ_E except for a proportionality constant γ.

$$U_i = \frac{\partial \psi_U}{\partial X_i} \tag{4.12}$$

Potentials ϕ_E and ψ_U satisfy the Cauchy-Riemann equations so that the fluid velocity U perpendicular to the electric field strength E at any position around the corners of the hole is:

$$U_i = \gamma E_j, \quad i \neq j \tag{4.13}$$

Equation (13) shows that those areas around the end corners of the hole, where a high electric field E causes a high rate of electrodeposition, will also be subject to a high rate of erosion because of a high fluid velocity U. Depending on the relative values of U and E (i.e., the value of the constant γ in Equation (4.13), net plating or net erosion can occur. In highly agitated solutions where γ is large, cases of net erosion have been observed in the through-hole plating of printed circuit boards (25). For the through-hole plating of 75 micron diameter holes in 330 micron thick SOS wafers, a to-and-from velocity of 4 cm/sec in the electroplating solution with a stroke length of 8 cm prevented plugging of the end of the holes, while at the same time, allowing some net plating to occur at these positions (see Figure 23).

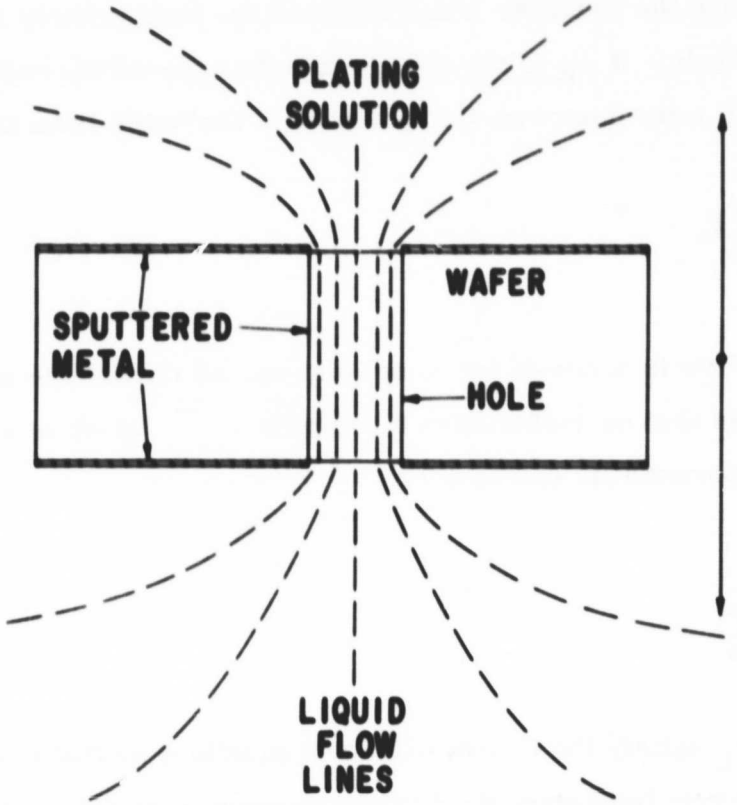


Figure 23. Through-hole electroplating of a double-sided-sputtered SOS wafer. To avoid plugging of the entrance and exit of the hole during electroplating, the wafer is moved to and fro so that the high electroplating rates induced by the high electrical fields at the entrance and exit edges of the hole are counterbalanced by the high erosion rates caused by liquid flow at these same locations.

It is interesting to estimate the actual average value of the fluid velocity in the laser-drilled hole that prevents hole plugging. The average fluid velocity U in the hole is related to the mass flow rate Q in the hole by

$$Q = U \pi D^2/_4 \tag{4.14}$$

where D is the diameter of the hole. The combination of Equations (4.1) and (4.14) yield

$$U = \frac{\Delta P\, D^2}{32\mu\, H} \tag{4.15}$$

where ΔP is the pressure differences between opposite sides of the laser-drilled hole, H is the length of the hole, and μ is the viscosity of the plating solution. The pressure differences ΔP across the wafer generated by its movement at a velocity V in the electroplating solution is

$$\Delta P = \frac{1}{2} \zeta V^2 \tag{4.16}$$

where ζ is the density of the solution. Equations (4.15) and (4.16) together give

$$U = \frac{\zeta V^2 D^2}{64 \mu H} \tag{4.17}$$

For typical values used in the present experiments of V = 4 cm/sec, $D = 7.5 \times 10^{-3}$ cm, $\mu/\zeta = 0.894$ cm^2/sec, $H = 3.30 \times 10^{-2}$ cm, the average velocity μ of the fluid in the laser-drilled hole is $U = 4.8 \times 10^{-4}$ cm/sec. Since the stroke length of the moving wafer is 8 cm, fluid moves into the hole for about 2 sec with the fluid velocity of 4.8×10^{-4} cm/sec to give an average fluid penetration length into the hole of about 10 microns, a number much smaller than one would intuitively guess. Nevertheless, this small average fluid velocity and fluid penetration length kept the laser-drilled holes opened during through-hole plating.

Higher wafer velocities led to excessive erosion rates at the end of the holes while lower velocities allowed the end of the holes to become rapidly plugged. Figure 24 shows a hollow feedthrough conductor in a laser-drilled hole in SOS after double-sided sputtering of one micron of gold and through-hole electroplating of 12 microns of copper. To-and-fro motion of 4 cm/sec of the wafer in the electroplating solution kept the entrance and exit of the hole open. Some signs of the erosion of the copper deposit by the fluid flow can be seen around the lip of the hole where the one micron film of gold has been partially uncovered and appears as a shiny, bright crescent in the microphotograph.

Hollow feedthrough holes made by double-sided sputtering and through-hole plating also make it possible to connect individual SOS wafers into a stacked array by a simple solder remelt technique. As shown in Figure 25, the metal fils on opposing faces of the wafers are first

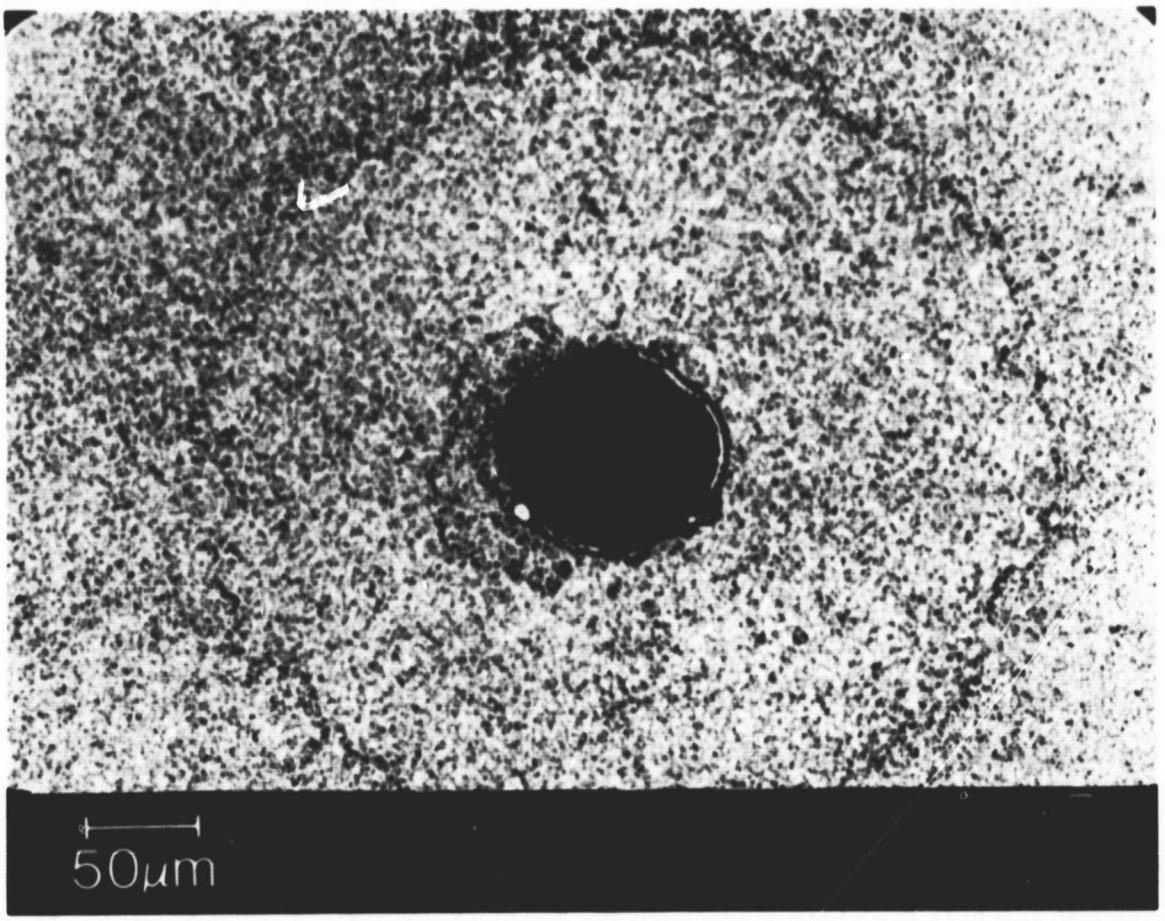


Figure 24. A hollow feedthrough conductor in a laser-drilled hole in SOS after double-sided sputtering of one micron of gold and through-hole plating of 12 microns of copper. To-and-fro motion of the wafer in the electroplating solution kept the entrance and exit of the hole open (500X).

stripped away. Figure 26 shows a photomicrograph of such a hole after stripping. The wafer is then dipped into a solder bath where capillary action draws solder into the hollow copper feedthrough conductor as depicted in Figure 25. To form an electrically-connected stacked array of SOS wafers, the SOS wafers with solder-filled feedthroughs are placed one on top of another so that the solder bumps of adjoining wafers are aligned (Figure 27). During a brief remelt, capillary forces cause the abutting solder bumps to flow together and form a conductive solder bridge between adjacent SOS wafers.

4.7 IMPLANTATION TECHNIQUES CONCLUSIONS

Both capillary wetting and wedge extrusion of a suspension of conductor particles into the laser-drilled holes in SOS wafers had two major problems with regard to use for the massively parallel processor. For commercially available conductor particle sizes, these methods

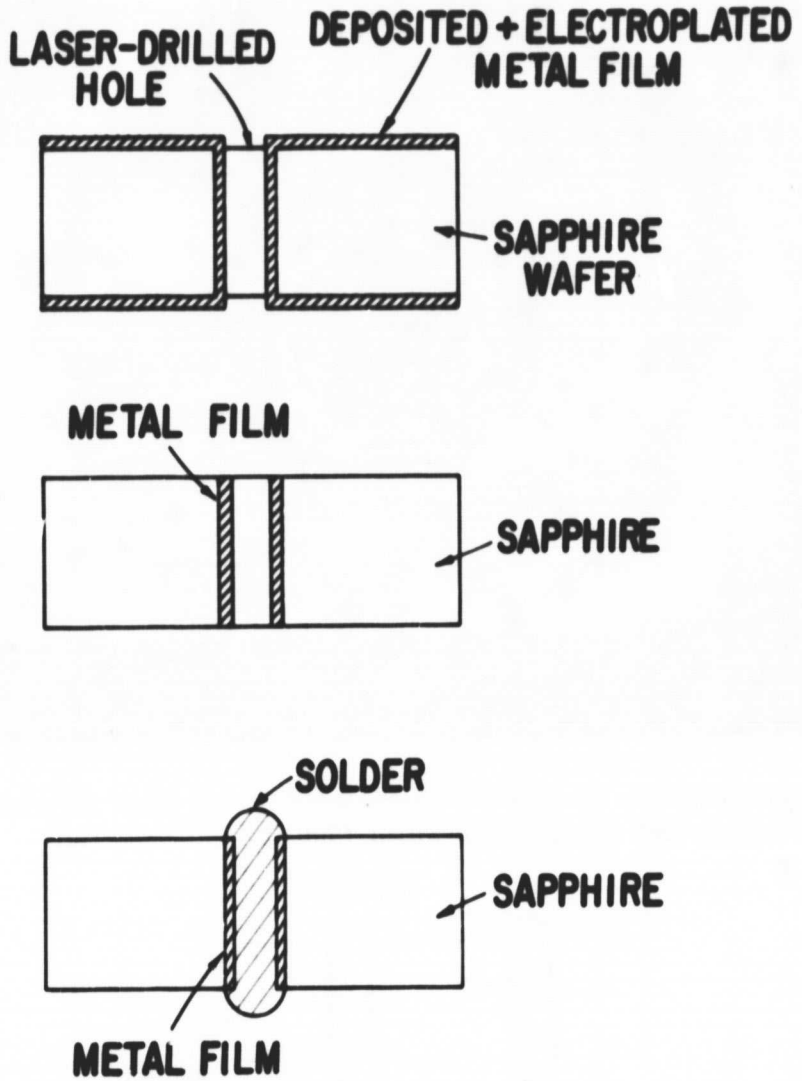


Figure 25. A hollow feedthrough conductor is filled with solder by first stripping away the metal film on opposing faces of the SOS wafer and then dipping the wafer into a solder bath where capillary action draws solder into the hollow metal feedthrough.

failed to fill holes smaller than 100 microns in diameter. The hole size is just on the edge of the range of hole sizes (less than 125 microns) that are useful for the massively parallel processor interconnects. In addition to the small-hole filling problem, a problem exists with the patterning of these conductor-filled liquids after they have been dried or cured. Normally, acid etches are used to pattern a pure metal film, while plasma etching can be used to pattern

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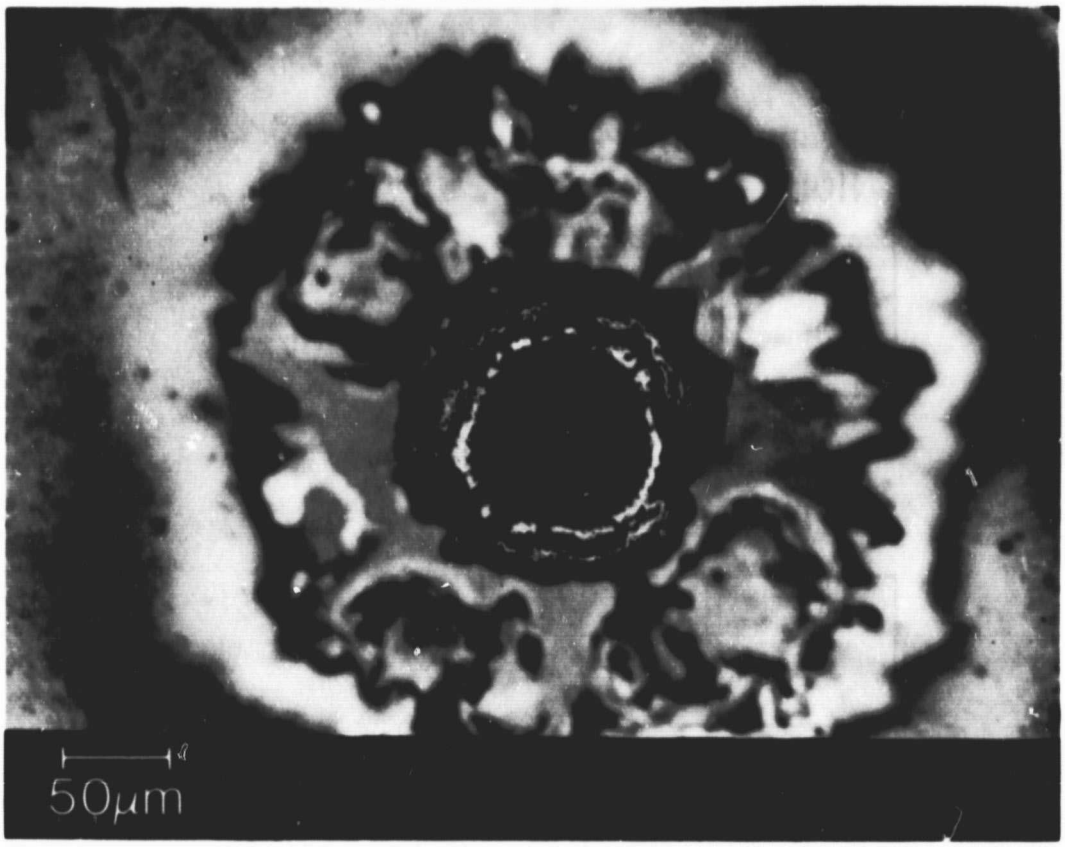

Figure 26. A photomicrograph of a hollow metal feedthrough after stripping away the metal film on both faces of the wafer (500X).

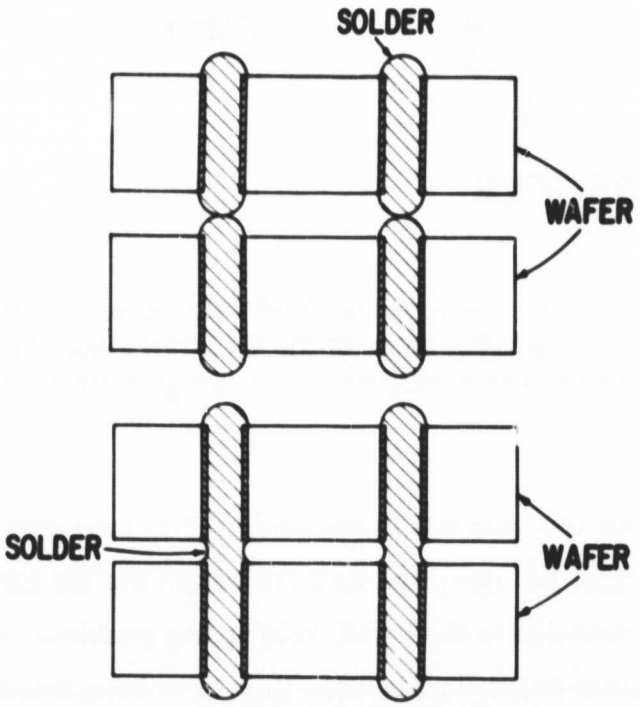

Figure 27. A schematic diagram of a method of forming an electrically-connected stacked array of SOS wafers with hollow, solder-filled feedthroughs by a brief remelt of abutting solder bumps.

an organic film. However, an organic film containing conducting metal particles cannot be patterned very well by either technique, and is, therefore, not compatible with current semiconductor processing technology.

Implantation of interconnects by wire insertion and electroplating is a good, dependable technique for small arrays containing less than a thousand holes. The wire interconnects provide a natural means of positioning the SOS wafers in a stacked array and the interconnect yield is high. For large arrays, however, this method is, at best, tedious, and is probably impossible for very large arrays such as the massively parallel processor, where one million interconnects are needed through each wafer.

Electroless plating is a simple, attractive method that with some concentrated development effort could become a practical means of providing electrical feedthroughs for the massively parallel processor. However, in the present investigation, through-hole yields were not high, since electroless plating was very erratic, probably because of the different surface conditions existing on laser-drilled sapphire as compared to surface-etched plastics for which electroless platting has been principally developed.

Electroforming provides good yields of implanted conductors, although the threat of current blockage by entrapped air bubbles in the laser-drilled holes is always present. The solid metal plugs formed by electroforming have the lowest electrical resistance of all the implants formed by the various methods. However, the different growth rates of individual implanted plugs during electroforming causes nonuniform plug sizes on the exit surface of the wafer. This nonuniformity can be alleviated by periodic reverse plating, but cannot be entirely eliminated. With a one million hole array, even a small standard deviation in implant sizes can be a serious problem. Finally, electroforming produces projecting bumps on the surface of the SOS wafer, which may prevent one from any further patterning of the surface by photolithographical techniques.

Of the six methods of implantation tried in this investigation, the double-sided sputtering and through-hole plating method achieved the best results. Implant yields were consistent 100%.

In addition, the wafer surfaces are flat and smooth following implantation by this method, so that a wafer can be subsequently processed with conventional semiconductor processing techniques. The electrical resistance of the implants is four orders of magnitude lower than the one ohm resistance specification for the massively parallel processor. Moreover, the hollow implant holes provided by this technique are available for a solder refill. These solder-refilled holes provide a natural way of forming an electrically connected stack of SOS wafers by abutting bumps of feedthroughs on adjacent wafers and briefly remelting the solder to form the desired connections.

SECTION 5

CUSTOM CMOS/SOS LSI TEST CIRCUIT

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A custom CMOS/SOS LSI type circuit was designed, layed out and fabricated to prove the feasibility and the limitations of drilling holes through sapphire substrates, and implanting conductive feed-throughs in these holes and connecting these substrate feed-throughs to active LSI circuitry on the top surface of the sapphire substrate. The basic purpose of the custom CMOS/SOS LSI circuit is to act as a test bed for the development of the conductive feed-throughs through the sapphire substrates. The design of this custom LSI circuit must be such that certain basic features and limitations of the conductive feed-throughs through sapphire can be demonstrated. These features and the limitations to be demonstrated are as follows:

1. Size limitations on holes and feed-throughs.
2. Minimum spacing that can be achieved between two feed-throughs adjacent to each other.
3. The minimum spacing of a conductive feed-through to an aluminum interconnect run on top of the substrate that would normally be used to interconnect devices in the LSI circuit.
4. The minimum spacing that can be achieved between a conductive feed-through and active CMOS circuitry on the surface of the substrate.

Figure 28 shows a layout diagram of the custom LSI CMOS/SOS circuit designed to demonstrate the above feed-through characteristics and limitations. There are basically two types of circuit on this custom LSI die. The most simple is the dog bone appearing type of circuitry where two feed-throughs are connected by surface aluminum interconnection run. These are shown positioned across the top rows and the bottom rows of the LSI layout in Figure 28. The second basic kind of circuit contains CMOS/SOS inverter buffer circuits. These are in the center rows of the die and are connected to feed-through type connections for both their input, and output. Power and ground buses run horizontally through the center of the circuit layout and have open pads for feed-throughs at two points along their length.

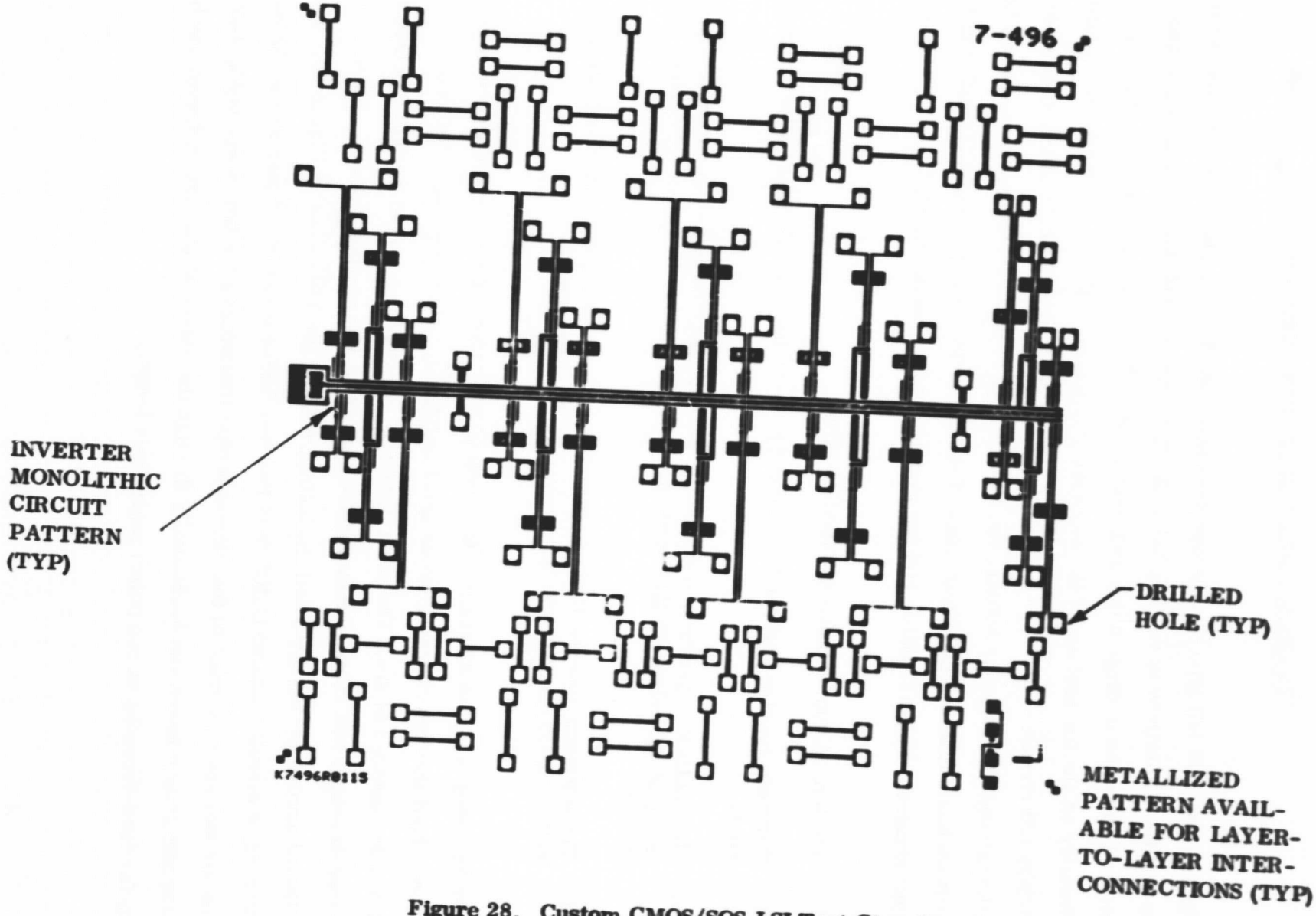

Figure 28. Custom CMOS/SOS LSI Test Circuit

Referring to the passive interconnects at the top rows and bottom rows of the die, Figure 28, it can be seen that a pair of feed-through holes is interconnected with a single aluminum run. The length of the interconnecting aluminum run between the feed-through holes is around 10 mils. The spacing between these feed-through holes is from 2 mils to 20 mils. It will also be noticed that to determine how close a feed-through can be to an aluminum run that some of the feed-through holes are in close proximity to aluminum runs and the spacing here varies from approximately 1 mil to 10 mils.

Looking at the center of the die, Figure 28, the horizontal lines running through the center are the VDD line and ground which connect to each of the CMOS inverters shown. Immediately above and below these horizontal power and ground lines are the CMOS inverters. All inverters have connected to them aluminum runs running vertically on the layout. These are the input/output connections to the circuit. These input/output connections are terminated in square pads that have an open area in the center for the drilling and implanting of the feed-through hole. The minimum spacings between these feed-throughs on the sapphire and the aluminum runs or the CMOS inverter or an adjacent feed-through is varied across the die from 0.5 mils spacing to 5 mils spacing.

The final experimental work during this program, in drilling through sapphire and implanting feed-throughs was done with the circuitry in the middle of the die containing the active CMOS inverters. The reason for this is that the center of the wafer contained all the types of elements and variations in proximity of these elements to provide the limitations of hole drilling spacings to each other and to aluminum interconnection runs and active circuitry. The patterns for the circuitry and square pads in the center of the die were designed to prove the three different points in feed-through implementation. These are: the minimum allowed spacing between drilled holes, demonstrated by the 6 CMOS/SOS inverter circuits at the far right of Figure 28. The minimum allowed spacing from drilled holes to aluminum runs, demonstrated in the middle left and right areas of the circuit. The minimum allowed spacing between a drilled hole and an active CMOS circuit without affecting circuit operation or conductive aluminum run integrity, demonstrated by the circuitry having feed-through holes across the center of the circuit.

An extra set of square pads is shown connected to the I/O lines of the CMOS inverters. These are for probing to determine CMOS inverter circuit operation. The pads for the feed-throughs, when the circuit is initially produced, are mostly empty space in the middle with an aluminum border around them. This would make probing very difficult because of the 1 to 2 mil wide aluminum edge around these pad areas. Ideally the pads for the feed-throughs would be round to conform to the roundness of the drilled holes. The easiest way to accomplish the rounding out of the hole in the center of the feed-through pad is to put small squares in the layout in the corners of the square opening. This will maximize the contact area between the feed-through metal at the surface of the sapphire with the aluminum metallization around the pad connecting to the aluminum run to the CMOS circuit.

This test CMOS/SOS LSI circuit was designed and laid out using computer graphics, Applicons, at Space Systems Division, Valley Forge, Pa. The mask for the circuit and the actual processing of the circuit was then accomplished at the GE Solid State Applications Operation in Syracuse, New York. Ten wafers were made without active silicon circuitry on them for experimental purposes. Five LSI wafers were made with active CMOS circuitry for laser drilling and filling of feed-throughs to demonstrate the process. Probe tests were performed on the CMOS inverter circuits to prove that they were working circuits using the solid pads on the I/O lines for the probe testing.

SECTION 6

RESULTS OF PROCESSING CONDUCTIVE FEED-THROUGHS IN THE CMOS/SOS LSI TEST CIRCUIT

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RESULTS OF PROCESSING CONDUCTIVE FEED-THROUGHS IN THE CMOS/SOS LSI TEST CIRCUIT

A lot of five Silicon-on-Sapphire (SOS) wafers with the test electronic circuits, test conductor runs and holes in aluminum pads for conductor feed-throughs was processed. These wafers were covered with a protective layer of glass and a layer of photo-resist. Windows were opened in the glass and photo-resist layers at points where holes were to be laser drilled through the wafer. Holes were then laser-drilled at these points and were enlarged to a standard 2 mil hole size by a laser reaming technique.

With these final wafers, a new twist to the sputtering technique was tried by sputtering two layers of metal onto the wafer. The first layer was NiCr which was used to form a tenacious bond with the sapphire substrate and to form a barrier layer between the aluminum runs and the second sputtered layer of gold. This barrier layer is advantageous if the wafer is to be later heated to high temperatures to prevent the formation of gold-aluminum intermetallic compounds more commonly known as the purple plague.

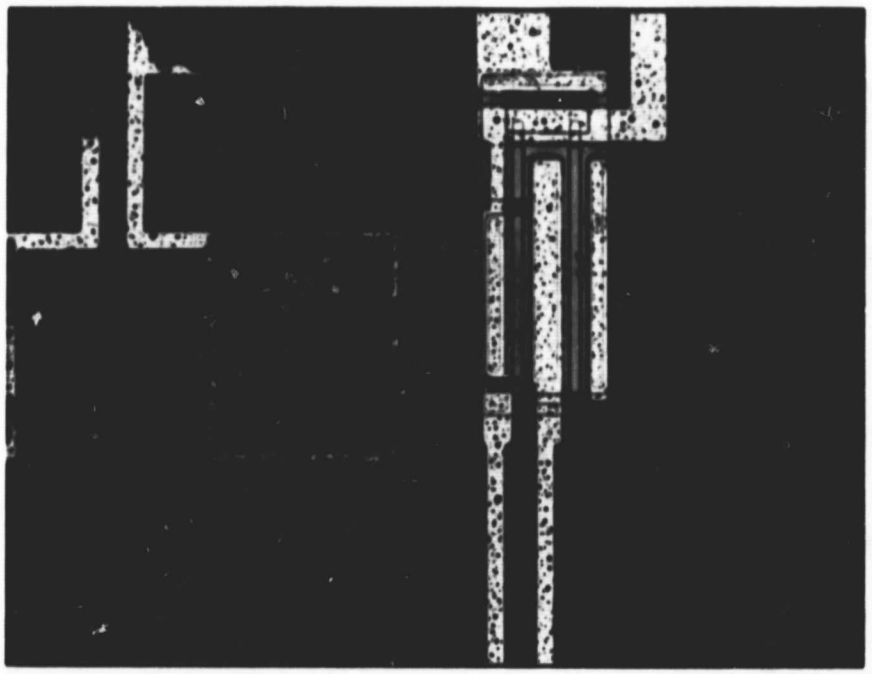
Following deposition of these layers on both sides of the wafer, the wafer was placed in an electroplating bath where a layer of copper was plated onto the wafers and into the laser-drilled holes.

The wafers were then sent to the photolighography unit to remove the sputtered and electro-plated metal on the major faces of the wafer. Previously, tests had been run with dummy wafers that showed that the sputtered and electroplated layers could be removed by a common photo-resist lift-off technique. With all of the experiments being run in parallel, this lift-off experiment was done with wafers that were laser-drilled with a lower powered laser than was used to drill the final wafers. Higher power laser drilling was developed to result in more consistent hold drilling. It was found with the final wafers that with higher power drilled laser holes some difficulty was experienced with the lift-off technique. The higher power laser, although resulting in more consistent hole drilling in sapphire, polymerized the photo-resist to such an extent that lift-off was difficult.

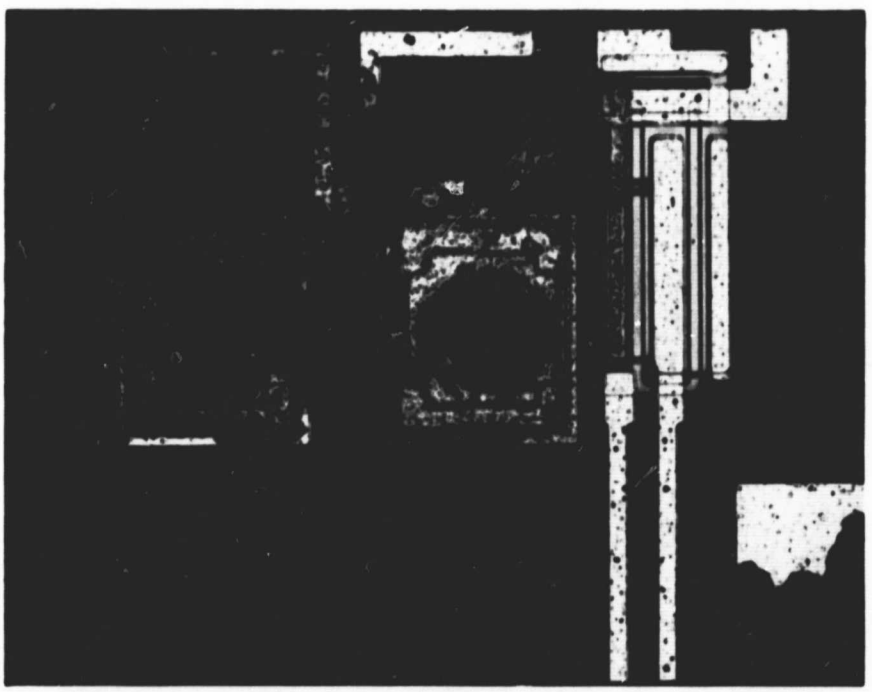
As a backup to photo-resist liftoff, removal of the metal from the wafer faces by selective etches was tried. The NiCr layer proved to be the Achilles heel of this effort since any etch that would remove NiCr also removed the underlying layer of Al, thereby damaging the pad connecting the feed-through to the Al run.

Figures 29 through 32 are pictures of the completed CMOS/SOS test circuit with and without the conductor feed-throughs completed from the circuit I/O pads to the reverse side of the sapphire.

Close inspection of the laser drilled holes with conductive feed-throughs show no existence of sapphire cracking in the vicinity of the hole. As a result even for feed-through holes within 0.5 mil of an active CMOS circuit or of an aluminum run there is no apparent effect on the circuit or the aluminum run. .



(a)

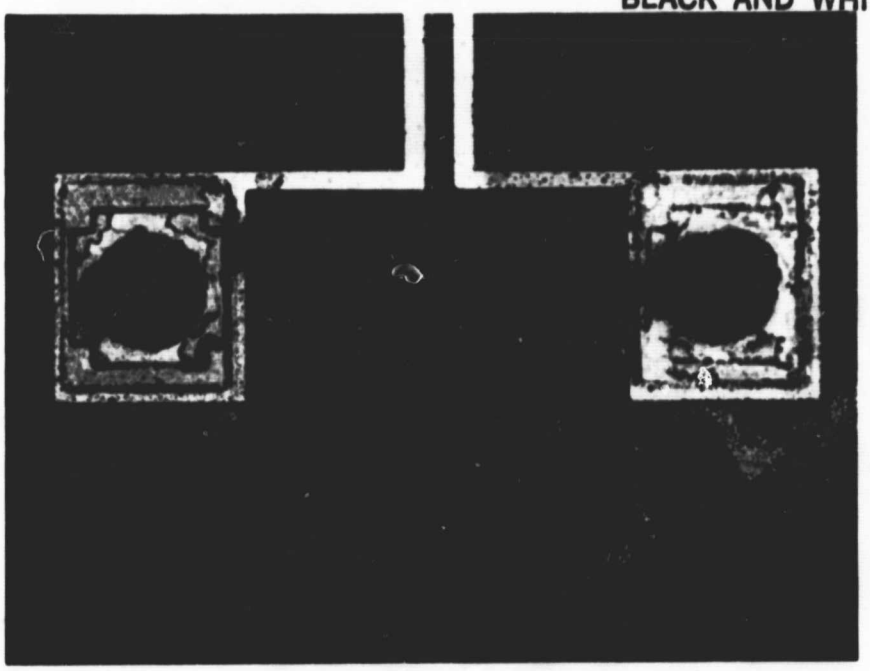


(b)

Note: Pads are 5 mils x 6 mils outside dimensions. Drilled holes are 3 mils in diameter inside a 4 mil pad opening, i.e., area devoid of aluminum.

Figure 29. (a) Single laser drilled hole implanted with conductive feed-through. Drilled pad is 2 mils from active CMOS inverter circuit; (b) Pair of laser drilled holes implanted with conductive feed-throughs. Spacing between feed-through pads is 2 mils. Spacing from feed-through pad to active CMOS inverter circuit is 0.5 mils.

(a)

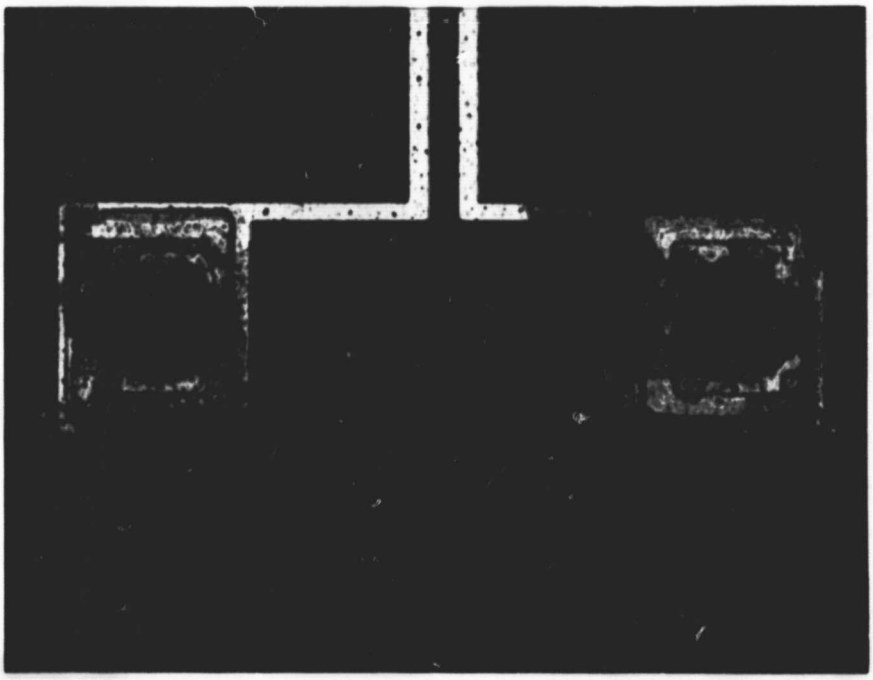


(b)

Note: Pads are 5 mils x 6 mils outside dimensions. Drilled hole diameters are 3 mil in 4 mil pad opening, i.e., area devoid of aluminum

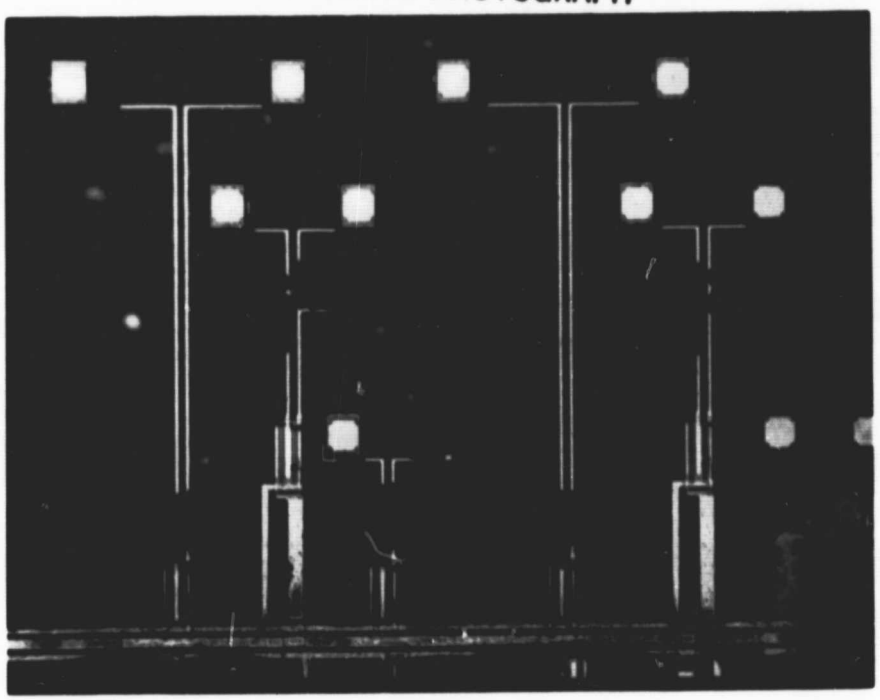
Figure 30. (a) Pair of laser drilled holes with conductive feed-throughs. Spacing between pads is 10 mils; (b) Pair of laser drilled holes with conductive feed-throughs. Spacing between holes is 10 mils.

(a)

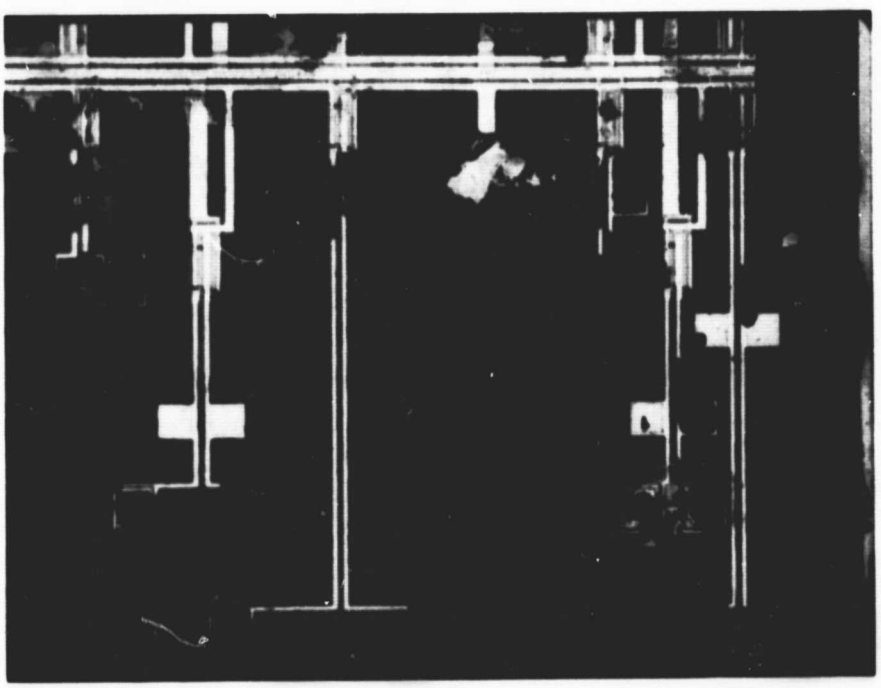


(b)

Figure 31. (a) Pair of laser drilled holes implanted with conductive feed-throughs. Spacing between feed-through pads is 5 mils. Spacing from edge of feed-through pad and CMOS inverter is 1 mil (200X magnification); (b) Pair of laser drilled holes with implanted conductive feed-throughs. Spacing between feed-through pads is 10 mils (200X magnification).



(a)



(b)

Figure 32. **(a) Section of custom CMOS/SOS die showing undrilled pads and circuitry (42X magnification); (b) Section of custom CMOS/SOS die showing laser drilled holes after conductive implantation. Note left side of picture shows spacing between completed feed-through pads and a CMOS inverter and between a completed feed-through pad and an aluminum run. These spacings are 0.5 mil, the minimum demonstrated (42X magnification).**

SECTION 7

CONCLUSIONS AND RECOMMENDATIONS

SECTION 7

CONCLUSIONS AND RECOMMENDATIONS

1. Techniques have been developed for successfully drilling feed-through holes through sapphire substrates for Silicon on Sapphire (SOS) LSI circuits.

2. Methods have been developed for drilling feed-through holes ranging from one to three mils in diameter through 13 mil thick SOS wafers. In addition, the ability to laser drill holes in the sapphire within less than 1 mil of aluminum runs and active CMOS circuitry has been demonstrated with no measurable spalling or cracking of the substrate. Also, no effect on the conductance of the aluminum run or on the CMOS inverter can be observed.

3. High conductance metal feed-throughs have been successfully implanted through the laser drilled holes in sapphire substrates.

4. These implantation techniques have been successfully demonstrated down to the 2 mil diameter hole size. Below this hole size, hole conductor implantation is erratic because wafer thickness to hole diameter exceeds a critical limit.

5. In the future NiCr layer can be eliminated since the wafer can be kept below temperatures where purple plague appears. Then with just a gold layer overlying an aluminum layer, the gold layer can be removed by a selective etch that does not attack the aluminum layer. Alternatively, an extra mask can be fabricated that will allow one to deposit a protective layer of photo-resist over the feed-through pad locations to protect them from etching when the sputtered metal film is being removed from the rest of the top and bottom surfaces of the SOS wafer.

6. The cumulative thickness of the metal layers deposited during sputtering and through-hole electroplating was found to impede conventional photo-resist lift-off techniques. Patterning and/or removal of these metal layers from the opposing major surfaces of the SOS wafer is best carried out by a photo-resist masking and etching technique or by a selective etching method.

SECTION 8

REFERENCES

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REFERENCES

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